

STF7N80K5, STFI7N80K5

Datasheet - production data

N-channel 800 V, 0.95 Ω typ., 6 A Zener-protected SuperMESH[™] 5 Power MOSFETs in TO-220FP and I²PAKFP packages

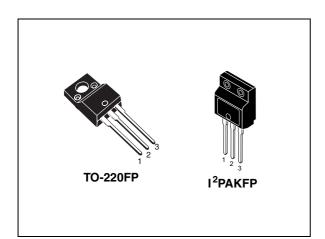
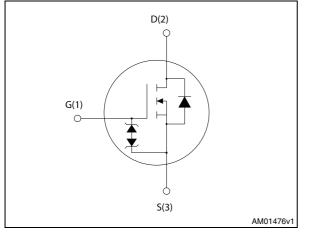


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	R _{DS(on)} max	I _D	P _{TOT}
STF7N80K5	800 V	100	6.4	
STFI7N80K5	800 V	1.2 Ω	6 A	25 W

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

• Switching applications

Description

These N-channel Zener-protected Power MOSFETs are designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH[™] 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Order codes	Marking	Package	Packaging
STF7N80K5	7N80K5	TO-220FP	Tube
STFI7N80K5	710015	I ² PAKFP	Tube

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This is information on a product in full production.

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1 Electrical ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate- source voltage	± 30	V
۱ _D	Drain current (continuous) at $T_C = 25 \ ^{\circ}C$	6 ⁽¹⁾	А
۱ _D	Drain current (continuous) at $T_C = 100 \ ^{\circ}C$	3.8 ⁽¹⁾	А
I _{DM} ⁽²⁾	Drain current (pulsed)	24 ⁽¹⁾	А
P _{TOT}	Total dissipation at $T_C = 25 \ ^{\circ}C$	25	W
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{jmax})	2	A
E _{AS}	Single pulse avalanche energy (starting $T_J = 25 \text{ °C}$, $I_D = I_{AS}$, $V_{DD} = 50 \text{ V}$)	88	mJ
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C =25 °C)	2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5	V/ns
Тj	Operating junction temperature	55 to 150	°C
T _{stg}	Storage temperature	-55 to 150	°C

Table 2.	Absolute	maximum	ratings
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1. Limited by package

2. Pulse width limited by safe operating area.

3. I_{SD} \leq 6 A, di/dt \leq 100 A/µs, V_{DS(peak)} \leq V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	5	°C/W
R _{thj-amb}	Thermal resistance junction-amb max	62.5	°C/W



2 Electrical characteristics

 $(T_{CASE} = 25 \ ^{\circ}C \text{ unless otherwise specified}).$

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 1 mA	800			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 800 V V _{DS} = 800 V, Tc=125 °C			1 50	μΑ μΑ
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100 \ \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 3 A		0.95	1.2	Ω

Table	4.	On/	/off	states
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Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} =100 V, f=1 MHz, V _{GS} =0	-	360	-	pF
C _{oss}	Output capacitance		-	30	-	pF
C _{rss}	Reverse transfer capacitance		-	1	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0$ to 640 V	-	47	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	20	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D =0	-	6	-	Ω
Qg	Total gate charge	V _{DD} = 640 V, I _D = 6 A	-	13.4	-	nC
Q _{gs}	Gate-source charge	V _{GS} =10 V	-	3.7	-	nC
Q _{gd}	Gate-drain charge	(see Figure 15)	-	7.5	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}



Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit			
t _{d(on)}	Turn-on delay time		-	11.3	-	ns			
t _r	Rise time	$V_{DD} = 400 V, I_D = 3 A, R_G=4.7 Ω, V_{GS}=10 V$ (see Figure 17)		8.3		ns			
t _{d(off)}	Turn-off delay time			23.7		ns			
t _f	Fall time			20.2		ns			

Table 6. Switching times

 Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		6	А
I _{SDM}	Source-drain current (pulsed)		-		24	А
$V_{SD}^{(1)}$	Forward on voltage	I _{SD} = 6 A, V _{GS} =0	-		1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 6 A, V _{DD} = 60 V	-	315		ns
Q _{rr}	Reverse recovery charge	di/dt = 100 A/µs,	-	2.8		μC
I _{RRM}	Reverse recovery current	(see Figure 16)	-	17.5		А
t _{rr}	Reverse recovery time	I _{SD} = 6 A,V _{DD} = 60 V	-	480		ns
Q _{rr}	Reverse recovery charge	di/dt=100 A/μs, _ Tj=150 °C	-	3.8		μC
I _{RRM}	Reverse recovery current	(see Figure 16)	-	16		А

1. Pulsed: pulse duration = $300\mu s$, duty cycle 1.5%

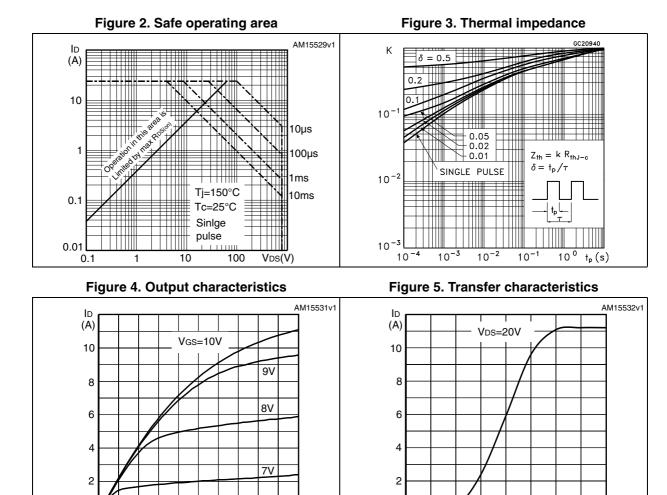
	Table 8.	. Gate-source Zener d	diode
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Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
V _{(BR)GSO}	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_{D} =0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.



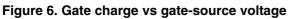
2.1 Electrical characteristics (curves)



6\

VDS(V)

16



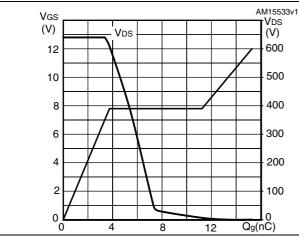
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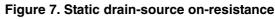
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4





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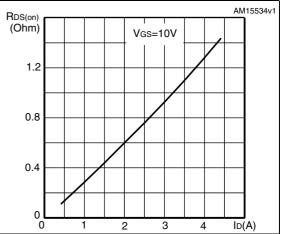
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VGS(V)

6

0

4



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Figure 8. Capacitance variations

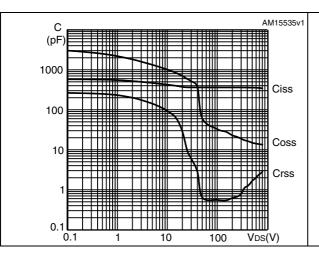


Figure 10. Normalized gate threshold voltage vs temperature

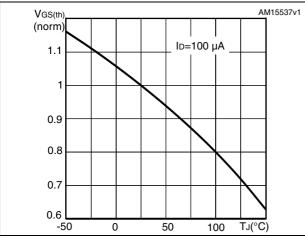


Figure 12. Normalized $\rm V_{(BR)DSS}$ vs temperature

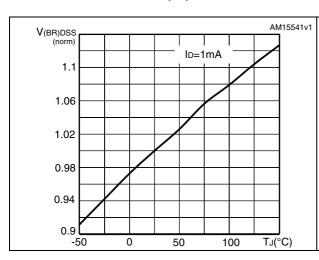
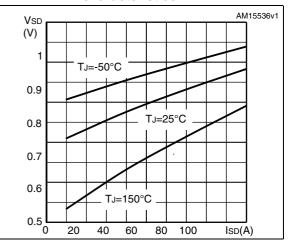
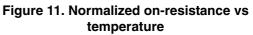


Figure 9. Source-drain diode forward characteristics





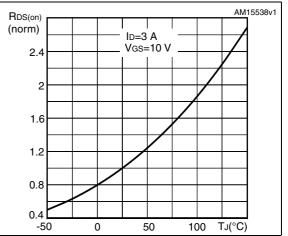
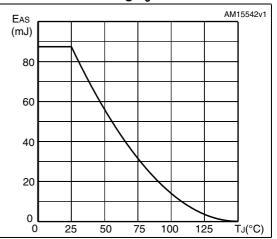


Figure 13. Maximum avalanche energy vs starting T_J





Test circuits 3

Figure 14. Switching times test circuit for resistive load

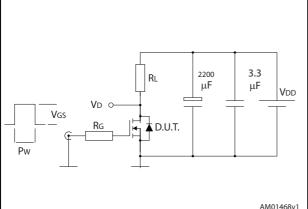


Figure 16. Test circuit for inductive load switching and diode recovery times

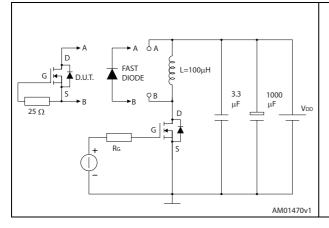


Figure 18. Unclamped inductive waveform

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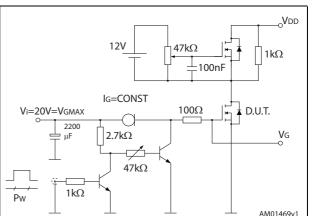
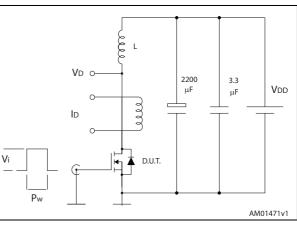
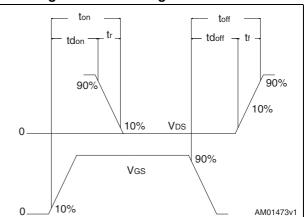


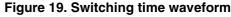
Figure 15. Gate charge test circuit

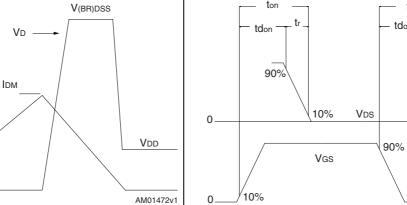












Vdd

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.



Table 9. TO-220FP mechanical data			
Dim.		mm	
	Min.	Тур.	Max.
A	4.4		4.6
В	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
Н	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Table 9. TO-220FP mechanical data



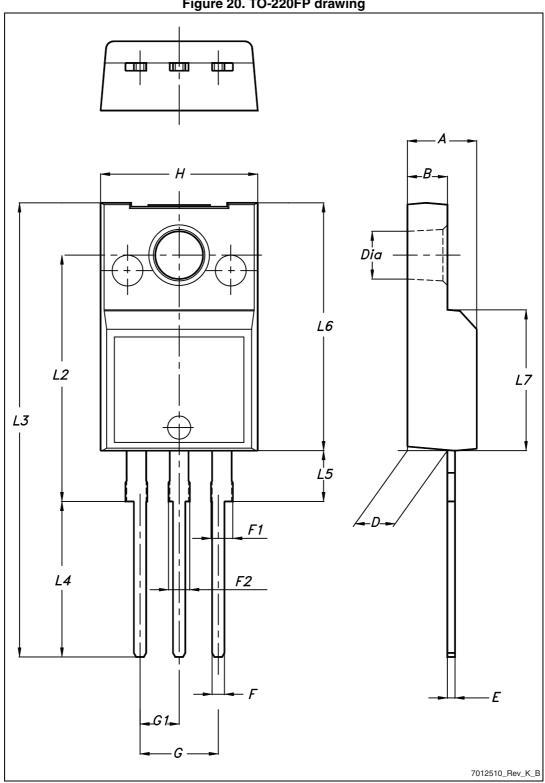


Figure 20. TO-220FP drawing

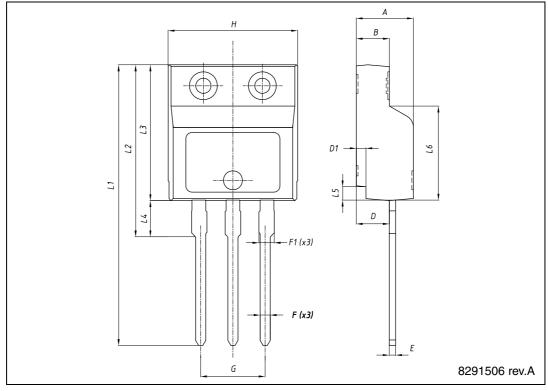


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Dim		mm	
Dim.	Min.	Тур.	Max.
А	4.40		4.60
В	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
Н	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

 Table 10.
 I²PAKFP (TO-281) mechanical data

Figure 21. I²PAKFP (TO-281) drawing





5 Revision history

Date	Revision	Changes
11-Oct-2013	1	First release. Part numbers previously included in datasheet DocID023448

Table 11. Document revision history



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