

N-channel 600 V, 0.115 Ω typ., 22 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data

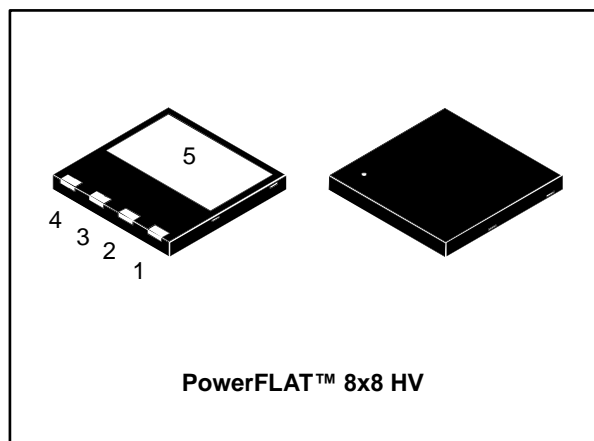
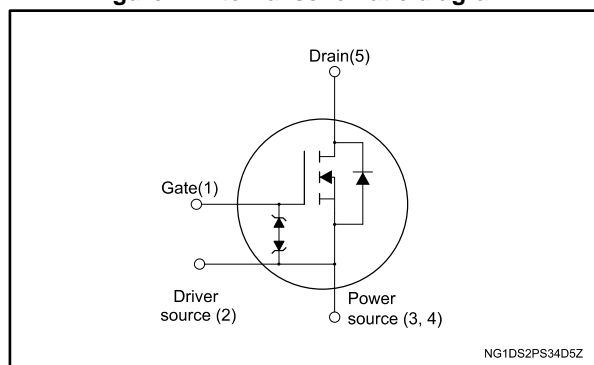


Figure 1: Internal schematic diagram



Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on)max}$	I_D
STL33N60M2	650 V	0.135 Ω	22 A

Features

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL33N60M2	33N60M2	PowerFLAT™ 8x8 HV	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	22	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	13.8	A
$I_{DM}^{(2)}$	Drain current (pulsed)	88	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	150	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	1100	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Operating junction temperature	150	°C

Notes:

(1)The value is limited by package.

(2)Pulse width limited by safe operating area.

(3) $I_{SD} \leq 22\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(\text{peak})} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

(4) $V_{DS} \leq 480\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	0.83	°C/W
$R_{thj\text{-amb}}^{(1)}$	Thermal resistance junction-ambient max	45	°C/W

Notes:

(1)When mounted on FR-4 board of inch^2 , 2oz Cu.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}, I_D = 11\text{ A}$		0.115	0.135	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	1781	-	pF
C_{oss}	Output capacitance		-	85	-	pF
C_{riss}	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0$	-	135	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	5.2	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 26\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 15: "Gate charge test circuit")	-	45.5	-	nC
Q_{gs}	Gate-source charge		-	9.9	-	nC
Q_{gd}	Gate-drain charge		-	18.5	-	nC

Notes:

⁽¹⁾ $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 13\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 14: "Switching times test circuit for resistive load")	-	16	-	ns
t_r	Rise time		-	9.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	109	-	ns
t_f	Fall time		-	9	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		22	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		88	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 26 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 26 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 17: "Unclamped inductive load test circuit")	-	375		ns
Q_{rr}	Reverse recovery charge		-	5.6		μC
I_{RRM}	Reverse recovery current		-	30		A
t_{rr}	Reverse recovery time	$I_{SD} = 26 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 17: "Unclamped inductive load test circuit")	-	478		ns
Q_{rr}	Reverse recovery charge		-	7.7		μC
I_{RRM}	Reverse recovery current		-	32.5		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.2 Electrical characteristics (curves)

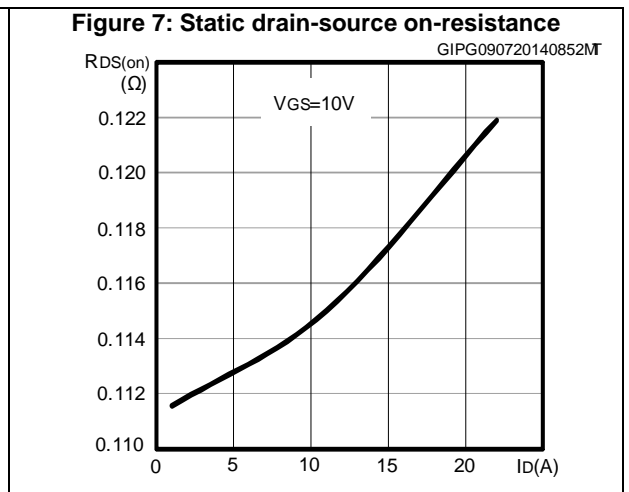
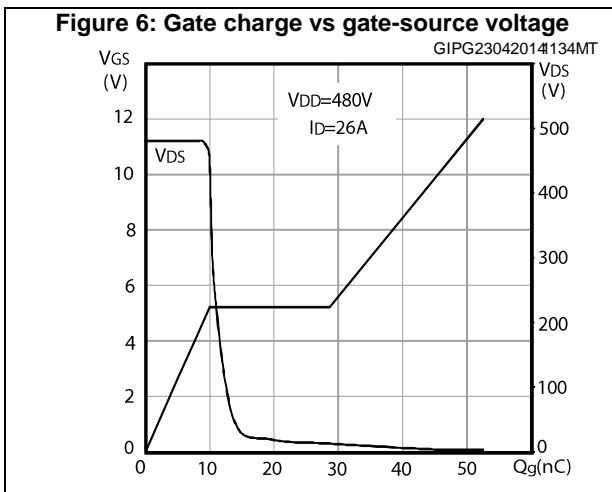
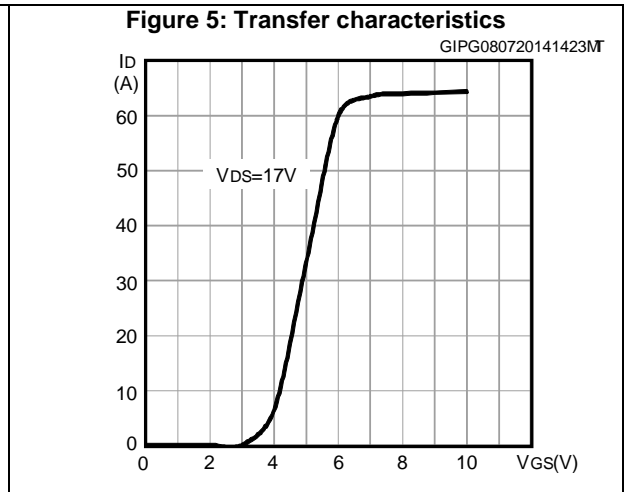
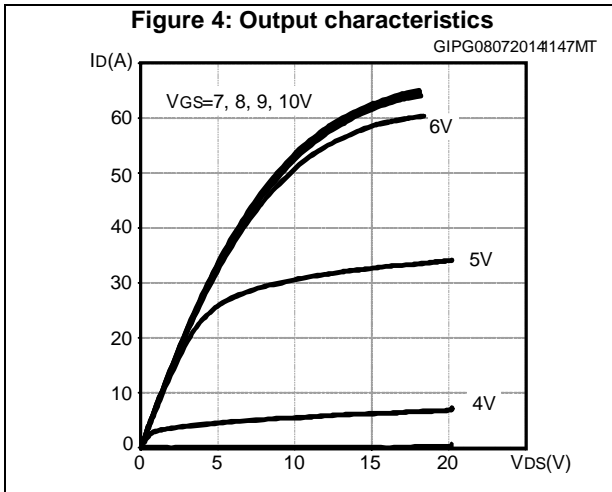
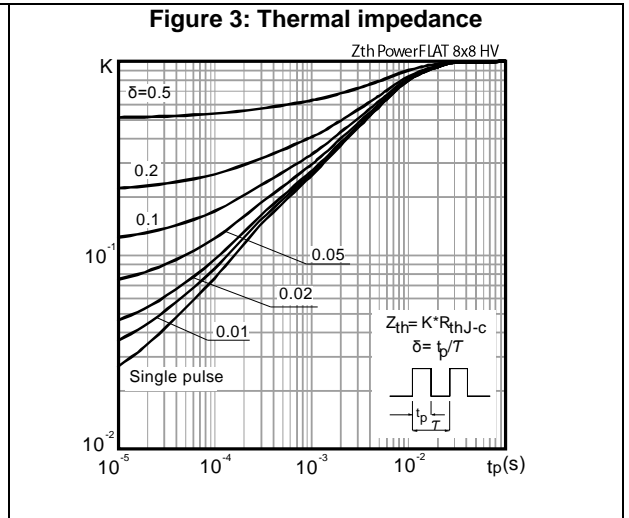
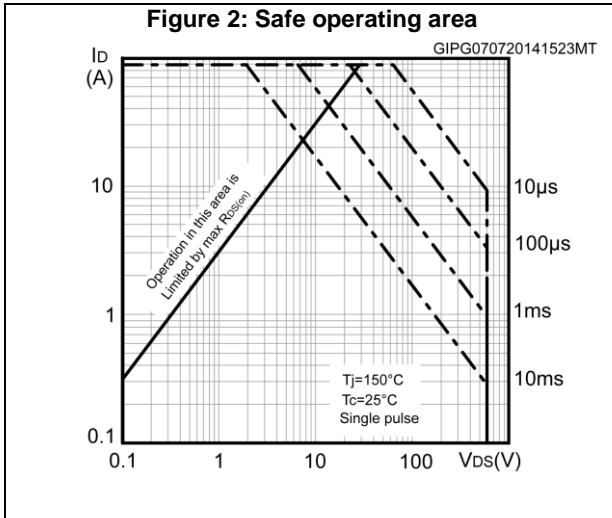


Figure 8: Capacitance variations

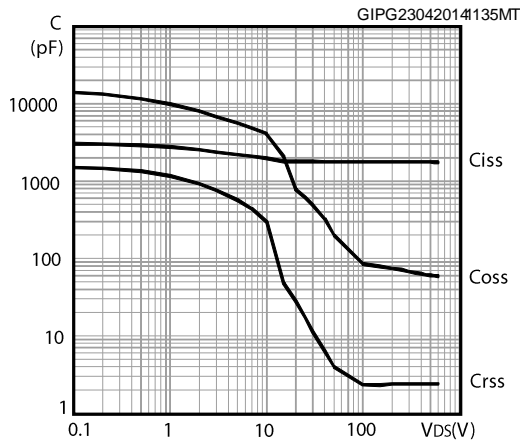


Figure 9: Normalized gate threshold voltage vs temperature

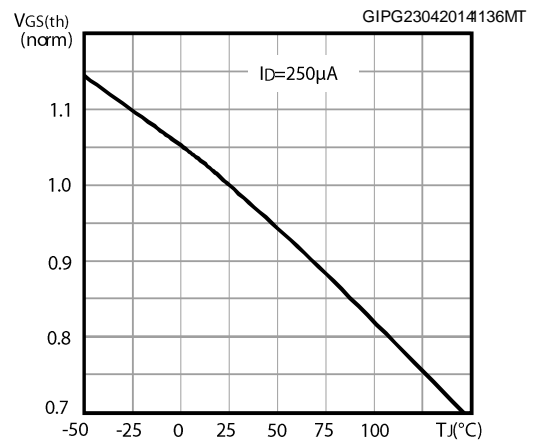


Figure 10: Normalized on-resistance vs temperature

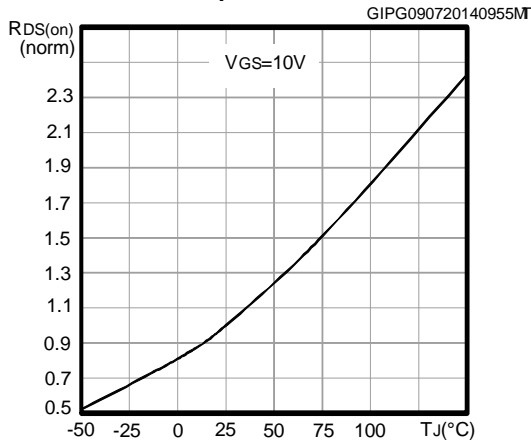


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

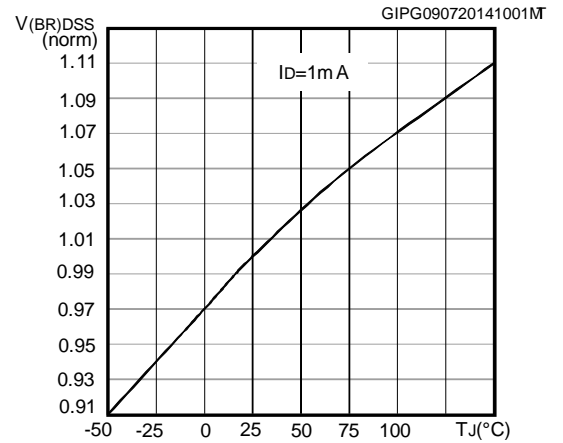


Figure 12: Source-drain diode forward characteristics

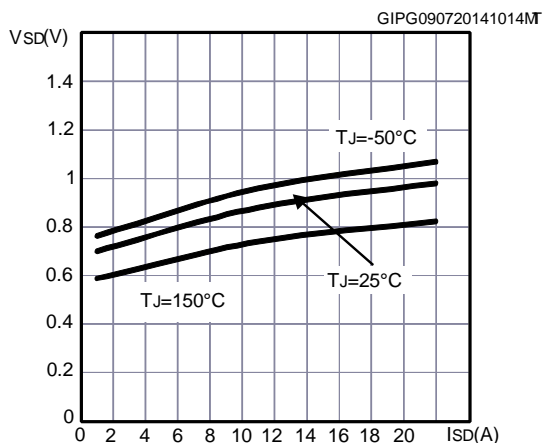
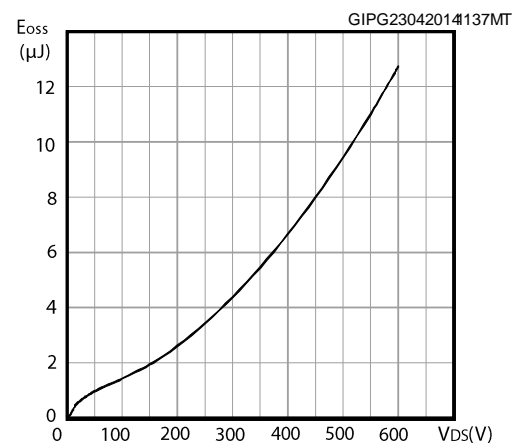
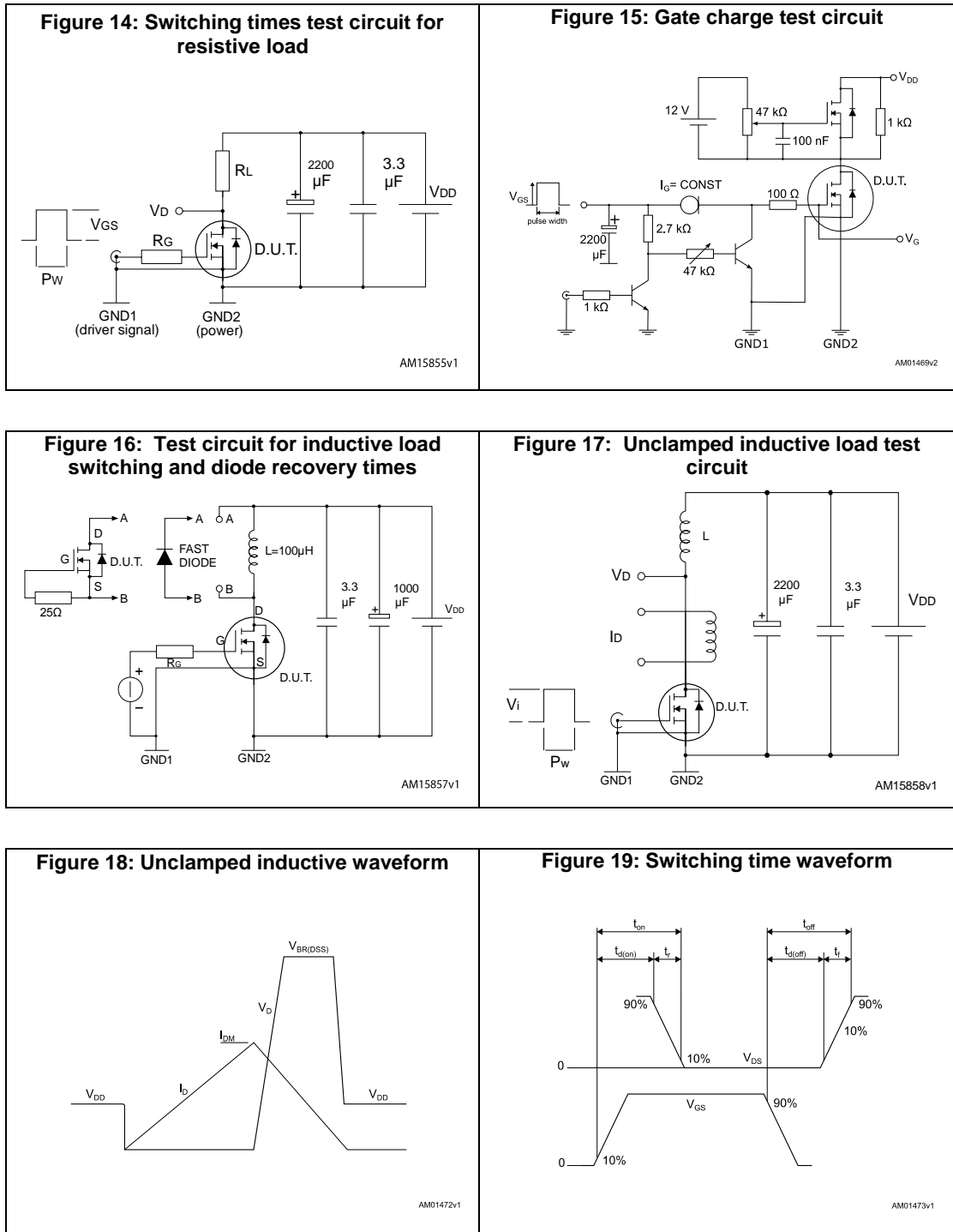


Figure 13: Output capacitance stored energy



3 Test circuits

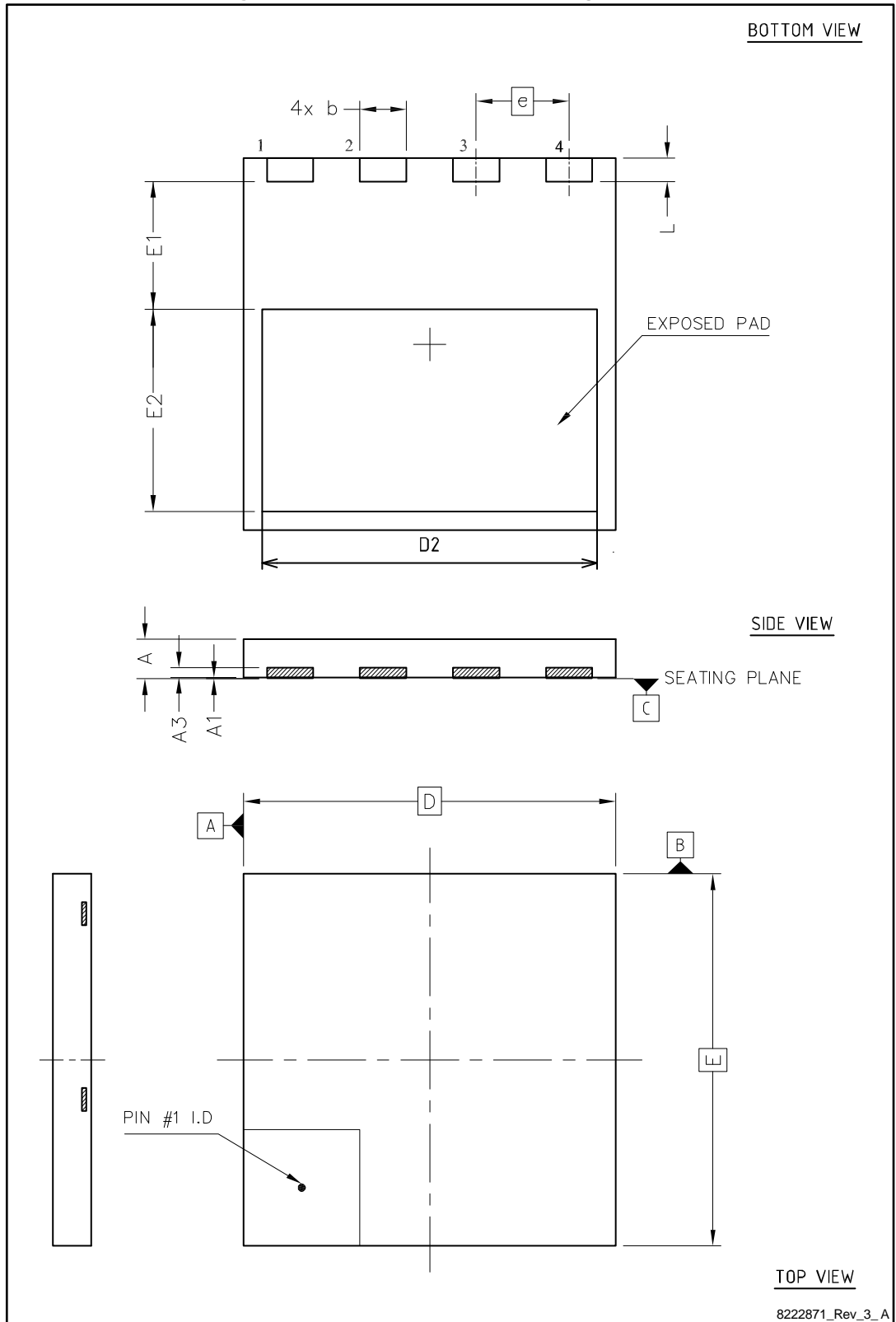


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT™ 8x8 HV package mechanical data

Figure 20: PowerFLAT™ 8x8 HV package outline

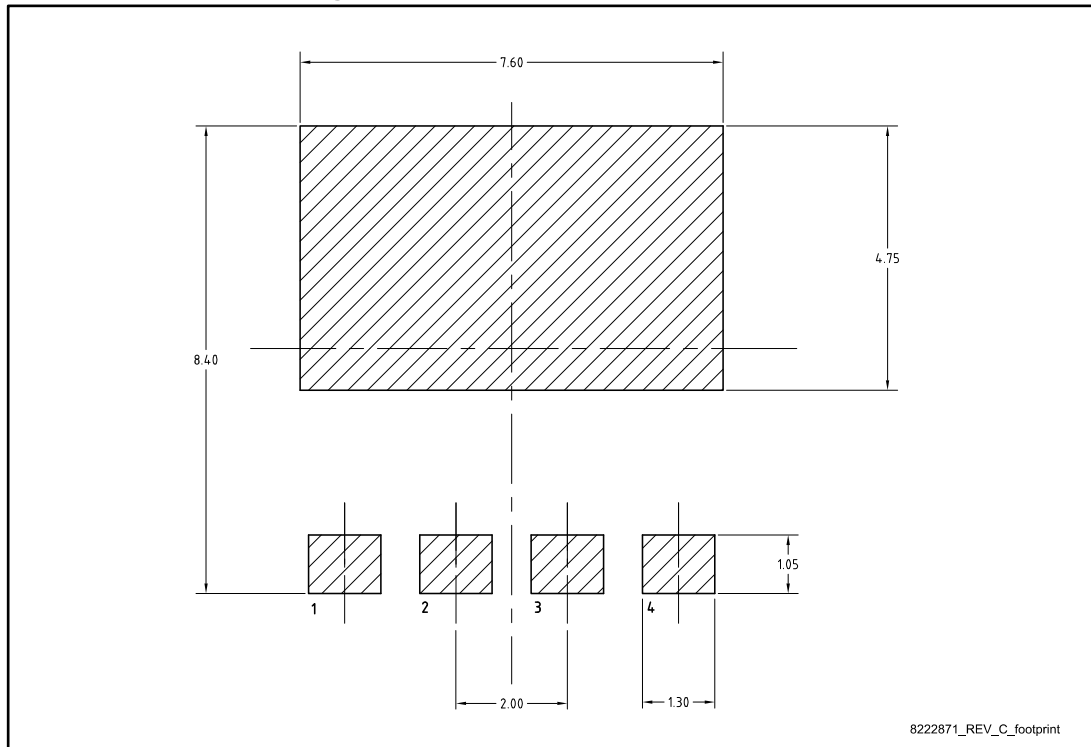


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Table 8: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

Figure 21: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

5 Packaging mechanical data

5.1 PowerFLAT™ 8x8 HV packaging mechanical data

Figure 22: PowerFLAT™ 8x8 HV tape

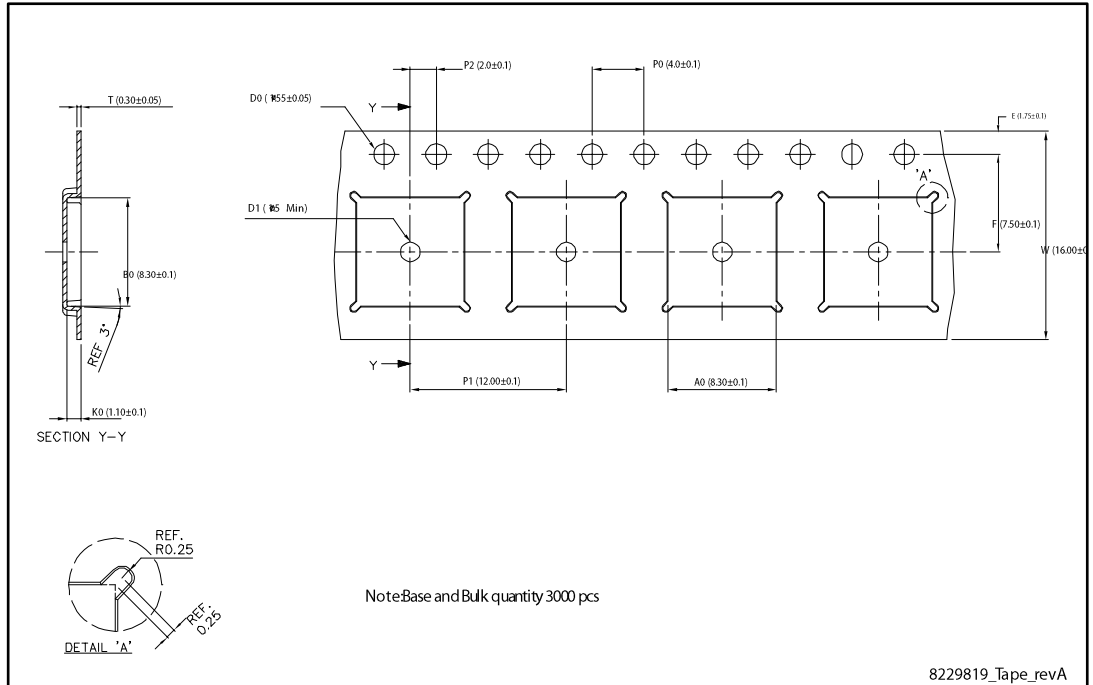


Figure 23: PowerFLAT™ 8x8 HV package orientation in carrier tape

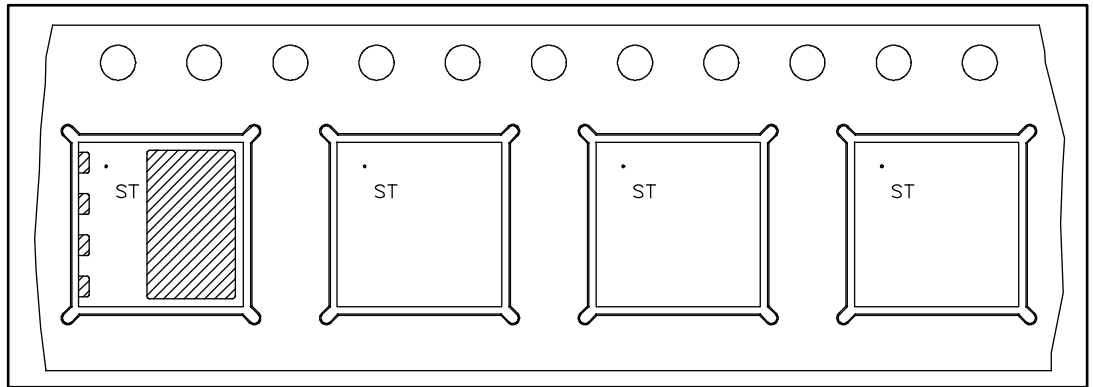
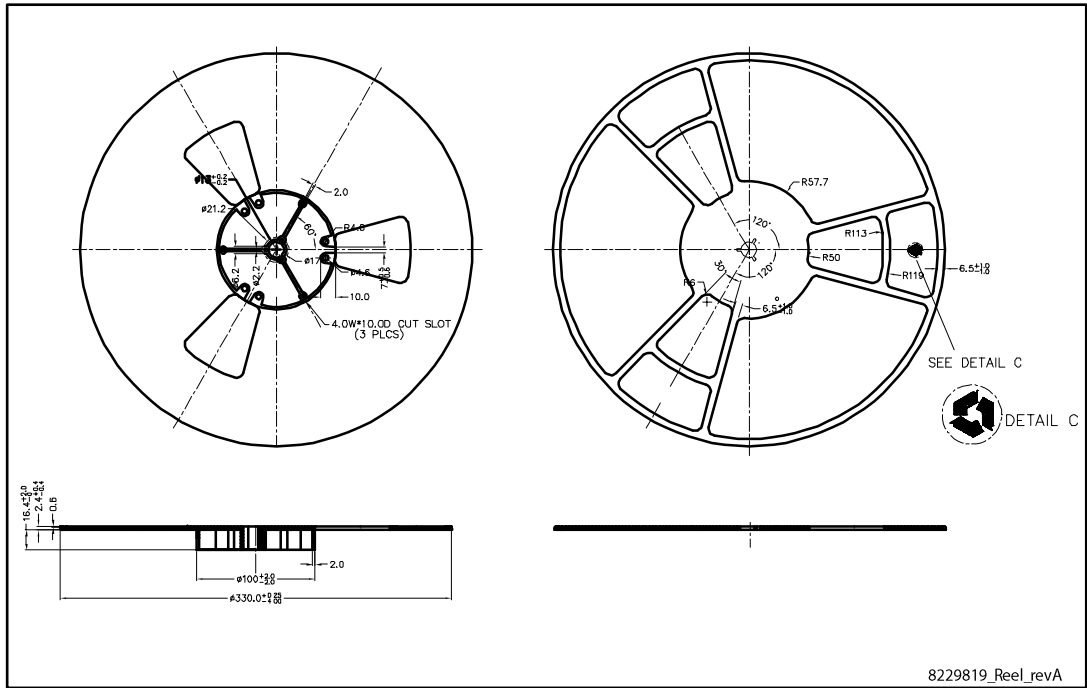


Figure 24: PowerFLAT™ 8x8 HV reel



6 Revision history

Table 9: Document revision history

Date	Revision	Changes
26-Jun-2013	1	First release.
23-Jul-2014	2	<p>Updated the title, the features and the description in cover page. Document status promoted from preliminary data to production data.</p> <p>Updated Figure 1: "Internal schematic diagram", Section 1: "Electrical ratings", Section 2: "Electrical characteristics".</p> <p>Added Section 2.1: "Electrical characteristics (curves)"</p> <p>Updated Section 3: "Test circuits", Section 4.1: "PowerFLAT™ 8x8 HV package mechanical data".</p>
20-Nov-2015	3	<p>Updated: cover image and <i>Figure 1: "Internal schematic diagram"</i> <i>Table 2: "Absolute maximum ratings"</i>, <i>Table 3: "Thermal data"</i> and <i>Table 6: "Switching times"</i></p> <p>Updated: <i>Figure 3: "Thermal impedance"</i></p> <p>Updated: <i>Section 5: "Test circuits"</i></p> <p>Updated: <i>Section 6.1: "PowerFLAT™ 8x8 HV package mechanical data"</i></p> <p>Minor text changes</p>

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