

### **STY60NM50**

# N-CHANNEL 500V - 0.045Ω - 60A Max247 Zener-Protected MDmesh™Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STY60NM50	500V	< 0.05Ω	60 A

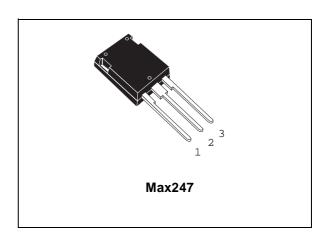
- TYPICAL  $R_{DS}(on) = 0.045\Omega$
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- IMPROVED ESD CAPABILITY
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL
- INDUSTRY'S LOWEST ON-RESISTANCE

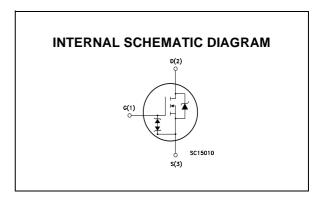


The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.



The MDmesh<sup>™</sup> family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.





#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	500	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	500	V
$V_{GS}$	Gate- source Voltage	±30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	60	Α
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	37.8	Α
I <sub>DM</sub> (•)	Drain Current (pulsed)	240	Α
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	560	W
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=15KΩ)	6	KV
	Derating Factor	4.5	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
Tj	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area November 2003

 $(1)I_{SD} \leq \!\! 60A, \ di/dt \leq \!\! 400A/\mu s, \ V_{DD} \leq V_{(BR)DSS}, \ T_j \leq T_{JMAX}$ 

#### **THERMAL DATA**

Ī	Rthj-case	Thermal Resistance Junction-case Max	0.22	°C/W
Ī	Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
	$T_I$	Maximum Lead Temperature For Soldering Purpose	300	°C

#### **AVALANCHE CHARACTERISTICS**

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max)	30	Α
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$ , $V_{DD} = 35$ V)	1.4	J

### **ELECTRICAL CHARACTERISTICS** (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	500			V
I <sub>DSS</sub>	Zero Gate Voltage	V <sub>DS</sub> = Max Rating			10	μA
	Drain Current (V <sub>GS</sub> = 0)	$V_{DS}$ = Max Rating, $T_{C}$ = 125 °C			100	μΑ
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			± 10	μA

### ON (1)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu A$	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 30A		0.045	0.05	Ω

## DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_{D} = 30A$		35		S
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		7500		pF
Coss	Output Capacitance			980		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			200		pF
R <sub>G</sub>	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.5		Ω

Note: 1. Pulsed: Pulse duration = 300  $\mu$ s, duty cycle 1.5 %.

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#### **ELECTRICAL CHARACTERISTICS** (CONTINUED)

#### **SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> = 250V, I <sub>D</sub> = 30A		51		ns
t <sub>r</sub>	Rise Time	$R_G = 4.7\Omega V_{GS} = 10V$ (see test circuit, Figure 3)		58		ns
Qg	Total Gate Charge	$V_{DD} = 400V, I_D = 60A,$		190	266	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10V		53		nC
$Q_{gd}$	Gate-Drain Charge			97		nC

#### **SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400V, I_{D} = 60A,$		51		ns
t <sub>f</sub>	Fall Time	$R_G = 4.7\Omega$ , $V_{GS} = 10V$ (see test circuit, Figure 5)		46		ns
t <sub>c</sub>	Cross-over Time	(See test sheart, Figure 5)		108		ns

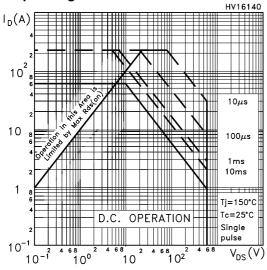
#### SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain Current				60	Α
I <sub>SDM</sub> (2)	Source-drain Current (pulsed)				240	Α
V <sub>SD</sub> (1)	Forward On Voltage	I <sub>SD</sub> = 60A, V <sub>GS</sub> = 0			1.5	V
t <sub>rr</sub> Q <sub>rr</sub> IRRM	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD}$ = 60A, di/dt = 100A/ $\mu$ s, $V_{DD}$ = 100 V, $T_j$ = 25°C (see test circuit, Figure 5)		532 9.9 37		ns µC A
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD}$ = 60A, di/dt = 100A/µs, $V_{DD}$ = 100 V, $T_j$ = 150°C (see test circuit, Figure 5)		636 13.4 42		ns µC A

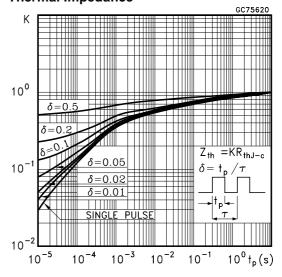
Note: 1. Pulsed: Pulse duration = 300  $\mu$ s, duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

#### **Safe Operating Area**

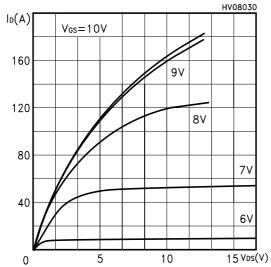


#### **Thermal Impedance**

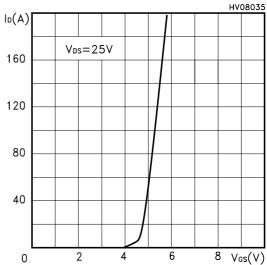


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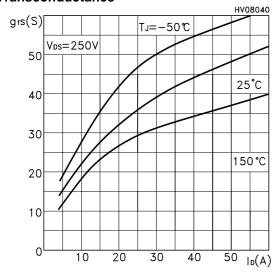
#### **Output Characteristics**



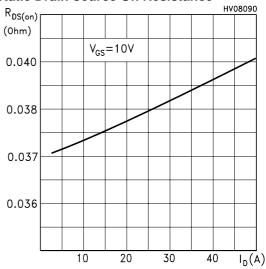
### Transfer Characteristics



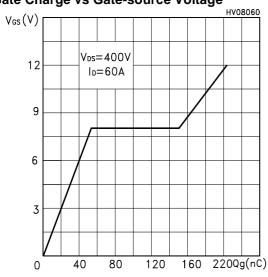
#### **Transconductance**



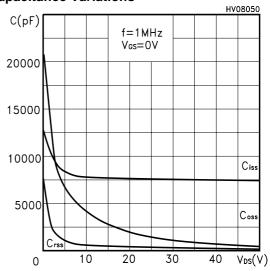
**Static Drain-source On Resistance** 



### **Gate Charge vs Gate-source Voltage**

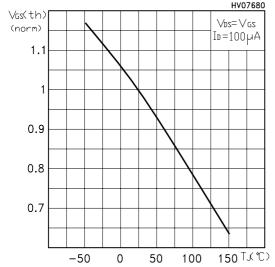


#### **Capacitance Variations**

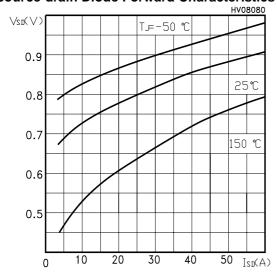


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## Normalized Gate Threshold Voltage vs Temp. $_{\rm HV07680}$



#### **Source-drain Diode Forward Characteristics**



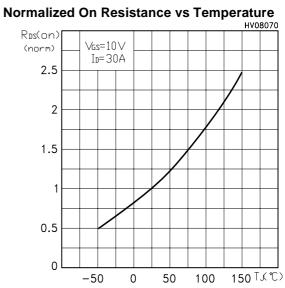


Fig. 1: Unclamped Inductive Load Test Circuit

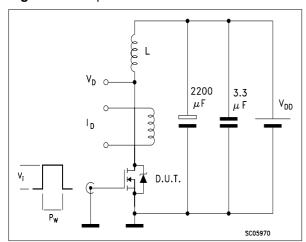


Fig. 3: Switching Times Test Circuit For Resistive Load

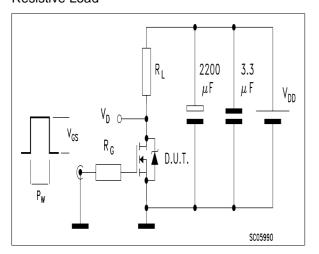


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

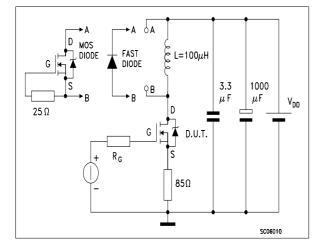


Fig. 2: Unclamped Inductive Waveform

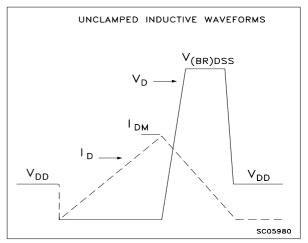
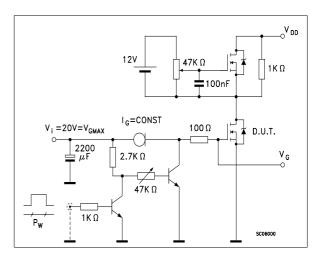


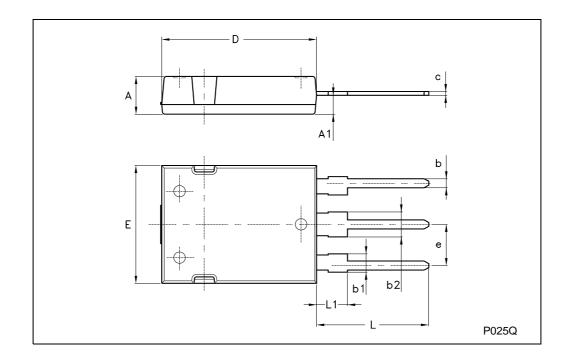
Fig. 4: Gate Charge test Circuit



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### **Max247 MECHANICAL DATA**

DIM.		mm		inch			
DIWI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Α	4.70		5.30				
A1	2.20		2.60				
b	1.00		1.40				
b1	2.00		2.40				
b2	3.00		3.40				
С	0.40		0.80				
D	19.70		20.30				
е	5.35		5.55				
E	15.30		15.90				
L	14.20		15.20				
L1	3.70		4.30				



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