



VN5E050MJ-E

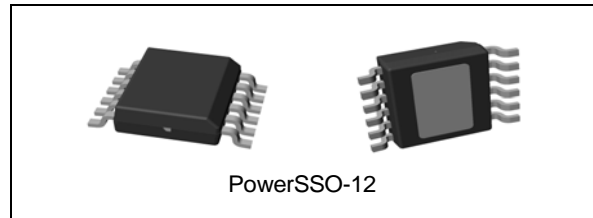
Single-channel high-side driver with analog current sense for automotive applications

Features

Max supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 V to 28V
Max on-state resistance	R_{ON}	50 m Ω
Current limitation (typ)	I_{LIMH}	27 A
Off-state supply current	I_S	2 $\mu A^{(1)}$

1. Typical value with all loads connected.

- General
 - Inrush current active management by power limitation
 - Very low standby current
 - 3.0 V CMOS compatible inputs
 - Optimized electromagnetic emissions
 - Very low electromagnetic susceptibility
 - In compliance with the 2002/95/EC european directive
 - Very low current sense leakage
- Diagnostic functions
 - Proportional load current sense
 - High current sense precision for wide currents range
 - Current sense disable
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients
 - Protection against loss of ground and loss of V_{CC}
 - Overtemperature shutdown with auto restart (thermal shutdown)
 - Reverse battery protected (see [Figure 29](#))



PowerSSO-12

- Electrostatic discharge protection

Application

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VN5E050MJ-E is a single channel high-side driver manufactured in the ST proprietary VIPower™ M0-5 technology and housed in the tiny PowerSSO-12 package. The VN5E050MJ-E is designed to drive 12 V automotive grounded loads delivering protection, diagnostics and easy 3 V and 5 V CMOS compatible interface with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel in order to provide Enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation and overtemperature indication.

The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS_DIS pin high to allow sharing of the external sense resistor with other similar devices.

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1 Block diagram and pin description

Figure 1. Block diagram

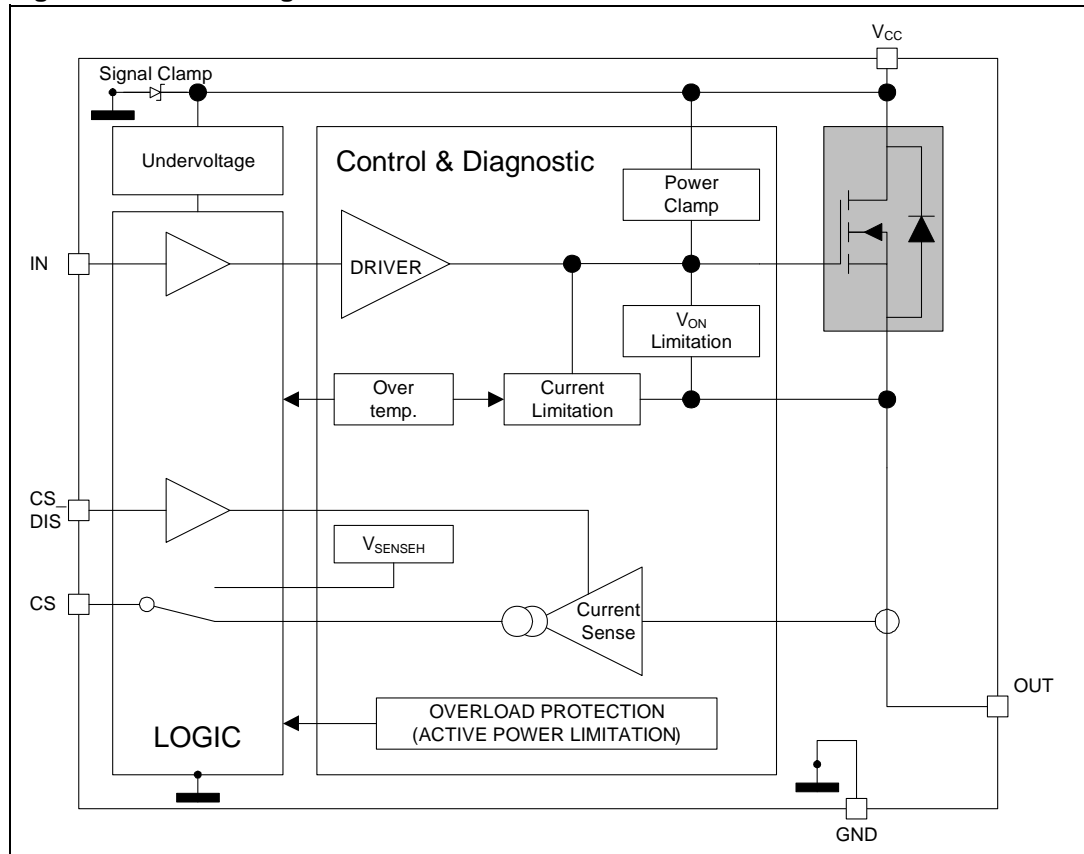


Table 1. Pin function

Name	Function
V _{CC}	Battery connection.
OUT	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
IN	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CS	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

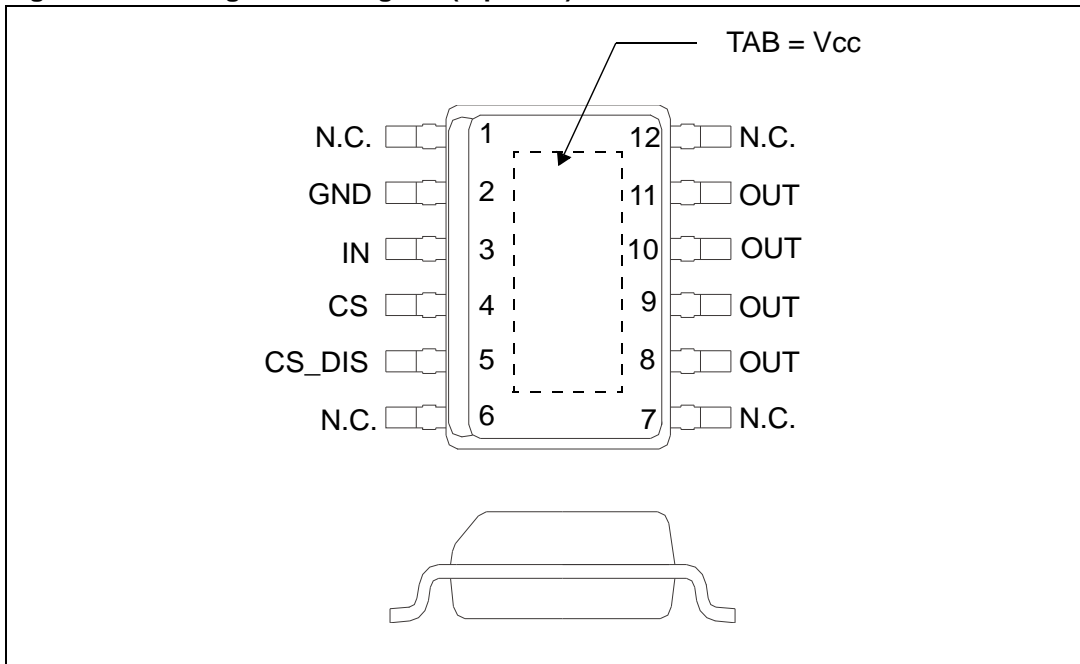
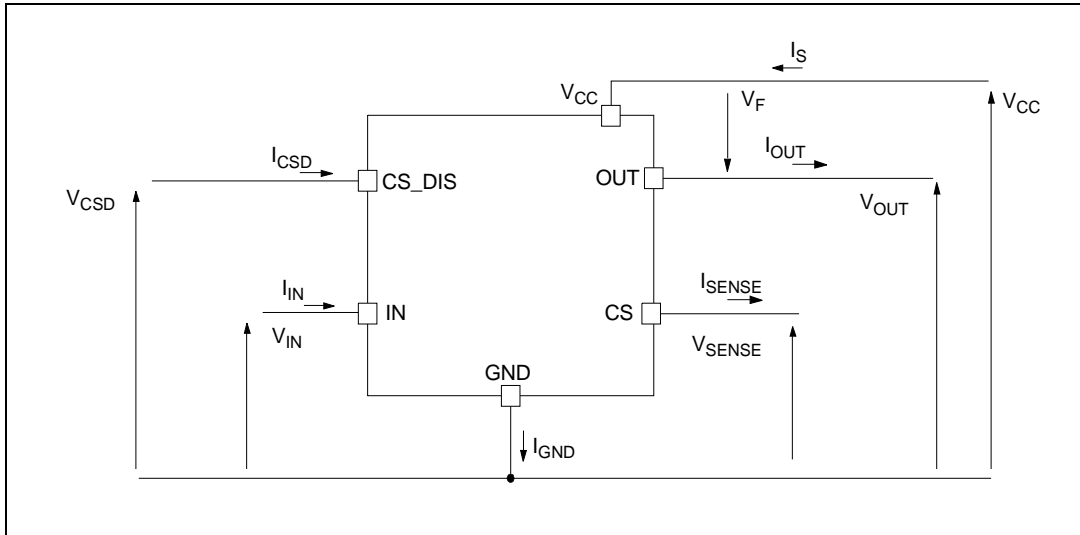


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 KΩ resistor	X	Through 22 KΩ resistor	Through 10 KΩ resistor	Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_F = V_{OUT} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	DC supply voltage	41	V
-V _{CC}	Reverse DC supply voltage	0.3	V
-I _{GND}	DC reverse ground pin current	200	mA
I _{OUT}	DC output current	Internally limited	A
-I _{OUT}	Reverse DC output current	20	A
I _{IN}	DC input current	-1 to 10	mA
I _{CS_DIS}	DC current sense disable input current	-1 to 10	mA
-I _{CSSENSE}	DC reverse CS pin current	200	mA
V _{CSSENSE}	Current sense maximum voltage	V _{CC} - 41 to +V _{CC}	V
E _{MAX}	Maximum switching energy (single pulse) (L = 3mH; R _L = 0Ω; V _{bat} = 13.5V; T _{jstart} = 150°C; I _{OUT} = I _{limL} (Typ.))	104	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V _{ESD}	Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF)		
	– INPUT	4000	V
	– CURRENT SENSE	2000	V
	– CS_DIS	4000	V
	– OUTPUT	5000	V
	– V _{CC}	5000	V
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _j	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
R _{thj-case}	Thermal resistance junction-case (with one channel ON)	2.7	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	See Figure 33	°C/W

2.3 Electrical characteristics

Values specified in this section are for $8V < V_{CC} < 28V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	$I_{OUT} = 2A$; $T_j = 25^{\circ}C$ $I_{OUT} = 2A$; $T_j = 150^{\circ}C$ $I_{OUT} = 2A$; $V_{CC} = 5V$; $T_j = 25^{\circ}C$			50 100 65	$m\Omega$ $m\Omega$ $m\Omega$
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}$	41	46	52	V
I_S	Supply current	Off-state; $V_{CC} = 13V$; $T_j = 25^{\circ}C$; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0V$ On-state; $V_{CC} = 13V$; $V_{IN} = 5V$; $I_{OUT} = 0A$		2 ⁽¹⁾ 1.5	5 ⁽¹⁾ 3	μA mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25^{\circ}C$ $V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}C$	0 0	0.01	3 5	μA
V_F	Output - V_{CC} diode voltage	$-I_{OUT} = 2A$; $T_j = 150^{\circ}C$			0.7	V

1. PowerMOS leakage included.

Table 6. Switching ($V_{CC} = 13V$; $T_j = 25^{\circ}C$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5\Omega$ (see Figure 5 .)	-	20	-	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5\Omega$ (see Figure 5 .)	-	40	-	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 6.5\Omega$	-	See Figure 23	-	$V/\mu s$
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 6.5\Omega$	-	See Figure 25	-	$V/\mu s$
W_{ON}	Switching energy losses during t_{on}	$R_L = 6.5\Omega$ (see Figure 5 .)	-	0.20	-	mJ
W_{OFF}	Switching energy losses during t_{off}	$R_L = 6.5\Omega$ (see Figure 5 .)	-	0.3	-	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN}=0.9V$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN}=2.1V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	5.5	-0.7	7	V V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	$V_{CSD}=0.9V$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD}=2.1V$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD}=1mA$ $I_{CSD}=-1mA$	5.5	-0.7	7	V V

Table 8. Protections and diagnostics (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	$V_{CC}=13V$ $5V < V_{CC} < 28V$	19	27	38 38	A A
I_{limL}	Short circuit current during thermal cycling	$V_{CC}=13V; T_R < T_J < T_{TSD}$		7		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}C$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}C$
T_{RS}	Thermal reset of status		135			$^{\circ}C$
T_{HYST}	Thermal hysteresis ($T_{TSD}-T_R$)			7		$^{\circ}C$
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT}=2A; V_{IN}=0; L=6mH$	$V_{CC}-41$	$V_{CC}-46$	$V_{CC}-52$	V
V_{ON}	Output voltage drop limitation	$I_{OUT}=0.1A;$ $T_J=-40^{\circ}C$ to $150^{\circ}C$ (see Figure 6)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8V<V_{CC}<18V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} =0.05A; V _{SENSE} =0.5V; V _{CSD} =0V; T _J = -40°C to 150°C	1170	2000	3090	
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 1A; V _{SENSE} =4 V; V _{CSD} =0V T _J = -40°C to 150°C T _J =25°C to 150°C	1575 1575	2000 2000	2750 2465	
dK ₁ /K ₁ (1)	Current sense ratio drift	I _{OUT} = 1A; V _{SENSE} = 4 V; V _{CSD} =0V; T _J = -40 °C to 150 °C	-10		10	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 2A; V _{SENSE} = 4V; V _{CSD} =0V; T _J = -40°C to 150°C T _J =25°C to 150°C	1765 1765	2000 2000	2315 2155	
dK ₂ /K ₂ (1)	Current sense ratio drift	I _{OUT} = 2A; V _{SENSE} = 4V; V _{CSD} =0V; T _J =-40 °C to 150 °C	-7		7	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 4A; V _{SENSE} =4V; V _{CSD} =0V; T _J = -40°C to 150°C T _J = 25°C to 150°C	1840 1840	2000 2000	2135 2080	
dK ₃ /K ₃ (1)	Current sense ratio drift	I _{OUT} = 4A; V _{SENSE} = 4 V; V _{CSD} =0V; T _J = -40 °C to 150 °C	-4		4	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} =0A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =0V; T _J =-40°C to 150°C V _{CSD} =0V; V _{IN} =5V; T _J =-40°C to 150°C I _{OUT} =2A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =5V; T _J =-40°C to 150°C	0 0		1 2	μA μA
I _{OL}	Open load on-state current detection threshold	V _{IN} = 5V, 8V<V _{CC} <18V I _{SENSE} = 5 μA	4		20	mA
V _{SENSE}	Max analog sense output voltage	I _{OUT} = 4A; V _{CSD} = 0V	5			V
V _{SENSEH}	Analog sense output voltage in fault condition ⁽²⁾	V _{CC} = 13V; R _{SENSE} = 3.9 KΩ		8		V
I _{SENSEH}	Analog sense output current in fault condition ⁽²⁾	V _{CC} = 13V; V _{SENSE} = 5V		9		mA
t _{DSENSE1H}	Delay response time from falling edge of CS_DIS pin	V _{SENSE} <4V, 0.5A<I _{OUT} <4A I _{SENSE} = 90% of I _{SENSE} max (see Figure 4.)		50	100	μs
t _{DSENSE1L}	Delay response time from rising edge of CS_DIS pin	V _{SENSE} < 4V, 0.5A<I _{OUT} <4A I _{SENSE} = 10% of I _{SENSE} max (see Figure 4.)		5	20	μs

Table 9. Current sense (8V<V_{CC}<18V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} < 4V, 0.5A<I _{out} <4A I _{SENSE} = 90% of I _{SENSE max} (see Figure 4.)		80	250	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4V, I _{SENSE} = 90% of I _{SENSEMAX} , I _{OUT} = 90% of I _{OUTMAX} I _{OUTMAX} = 2A (see Figure 7)			40	μs
t _{DSENSE2L}	Delay response time from falling edge of INPUT pin	V _{SENSE} < 4V, 0.5A<I _{out} <4A I _{SENSE} = 10% of I _{SENSE max} (see Figure 4.)		100	250	μs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation and overtemperature.

Figure 4. Current sense delay characteristics

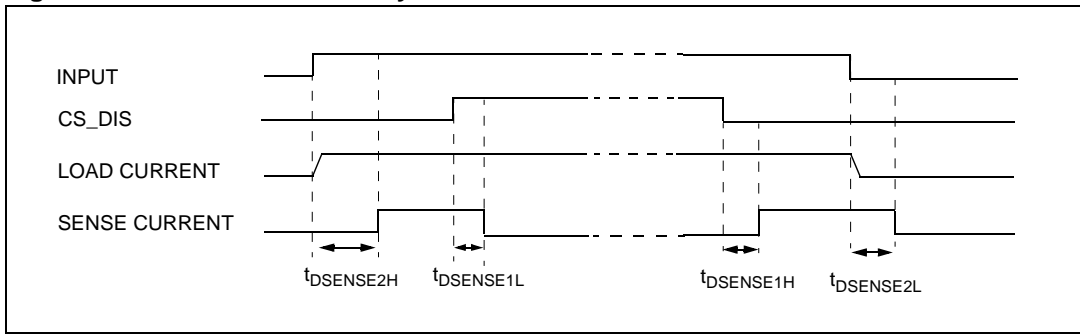


Figure 5. Switching characteristics

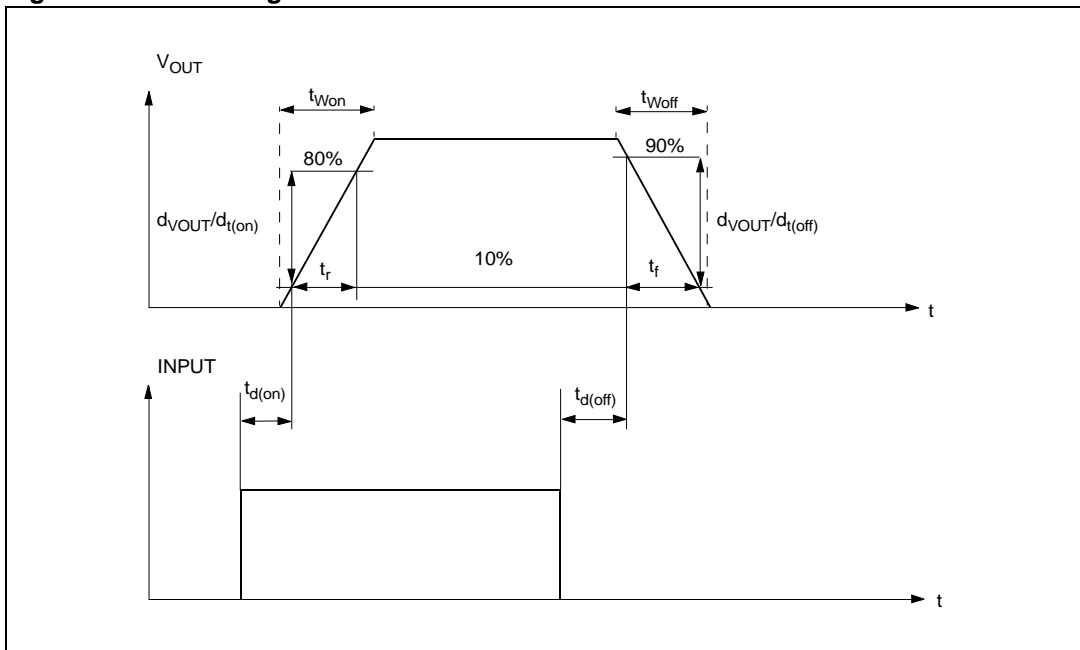


Figure 6. Output voltage drop limitation

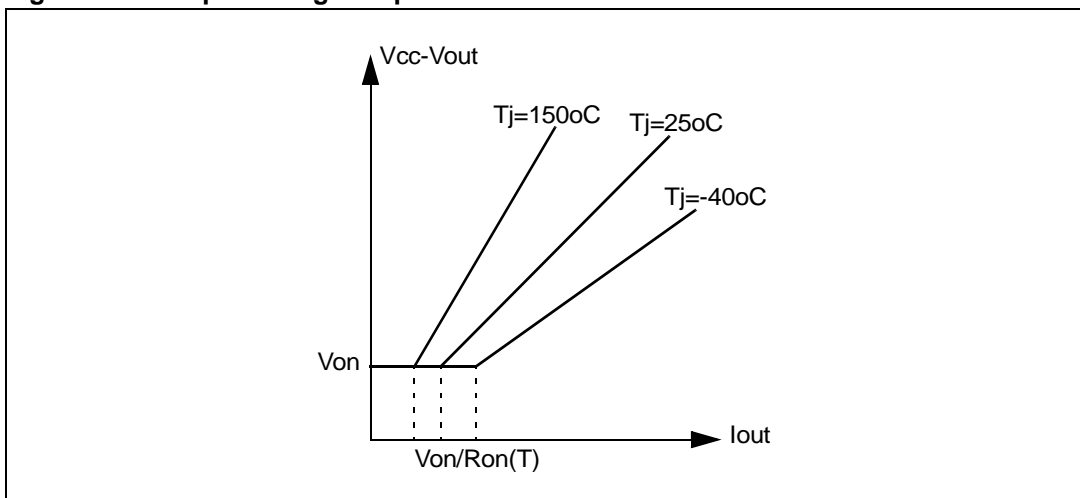


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

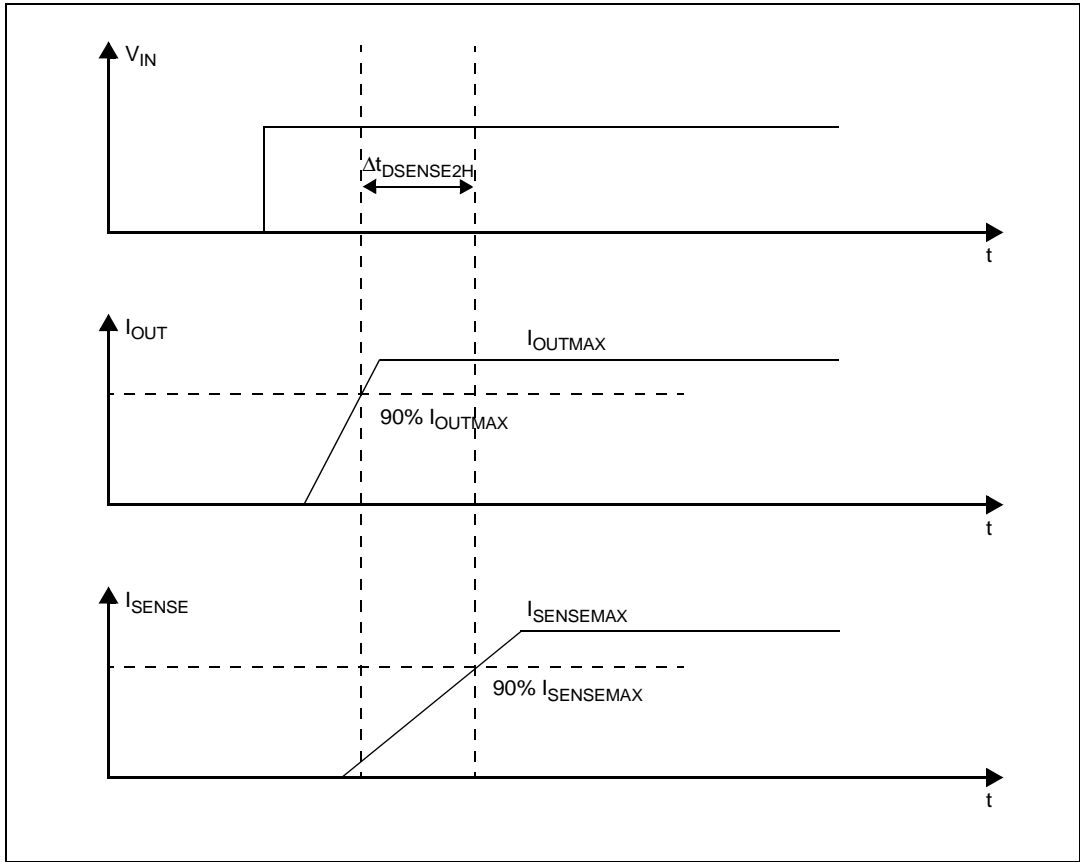


Figure 8. I_{OUT}/I_{SENSE} vs. I_{OUT}

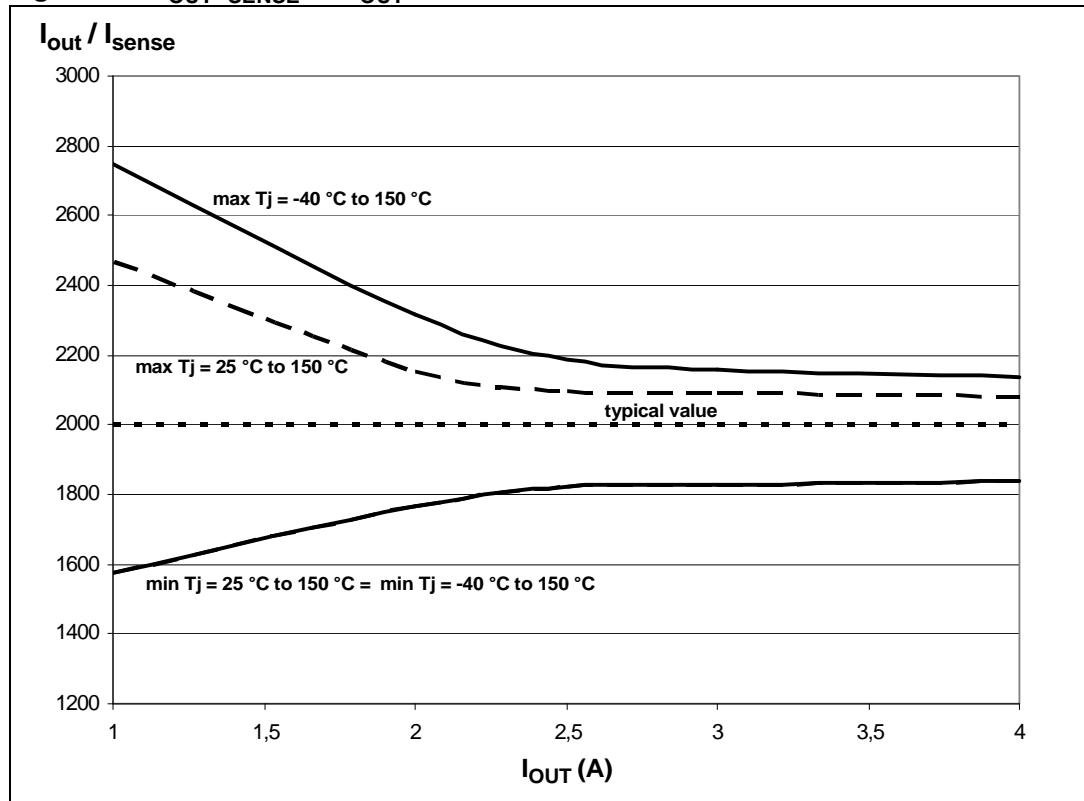
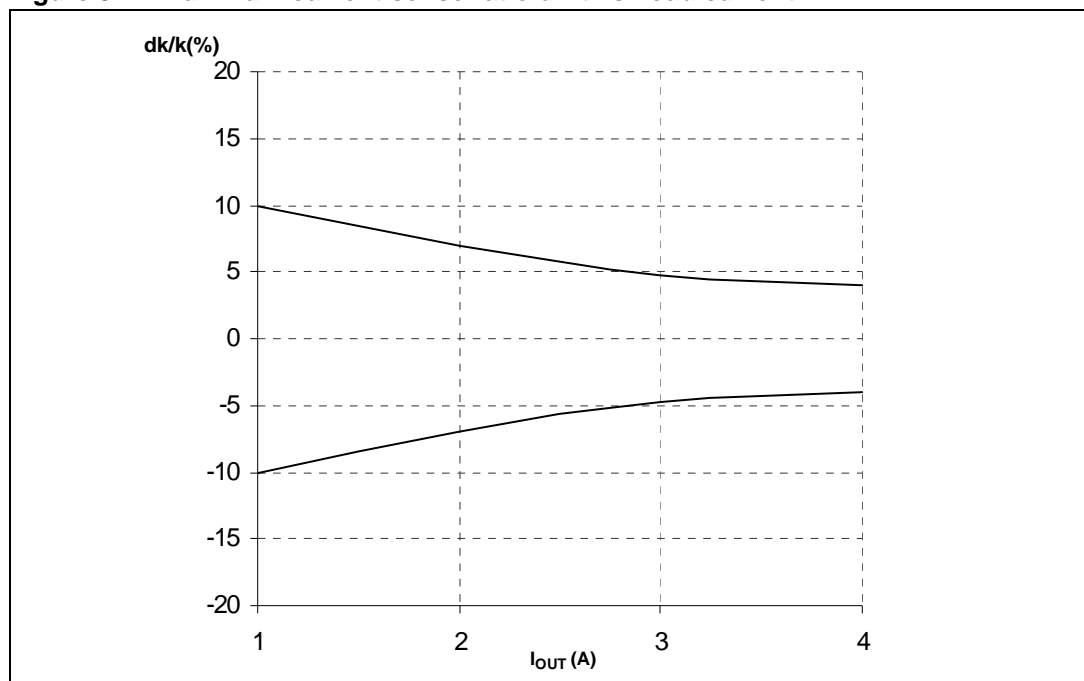


Figure 9. Maximum current sense ratio drift vs. load current



Note: Parameter guaranteed by design; it is not tested.

Table 10. Truth table

Conditions	Input	Output	Sense ($V_{CSD} = 0V$) ⁽¹⁾
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overload	H	X (no power limitation)	Nominal
	H	Cycling (power limitation)	V_{SENSEH}
Short circuit to GND (power limitation)	L	L	0
	H	L	V_{SENSEH}
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 11. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50μs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1μs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1μs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b ⁽²⁾	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b.
2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 12. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽²⁾	C	C

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b
2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 13. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 10. Normal operation

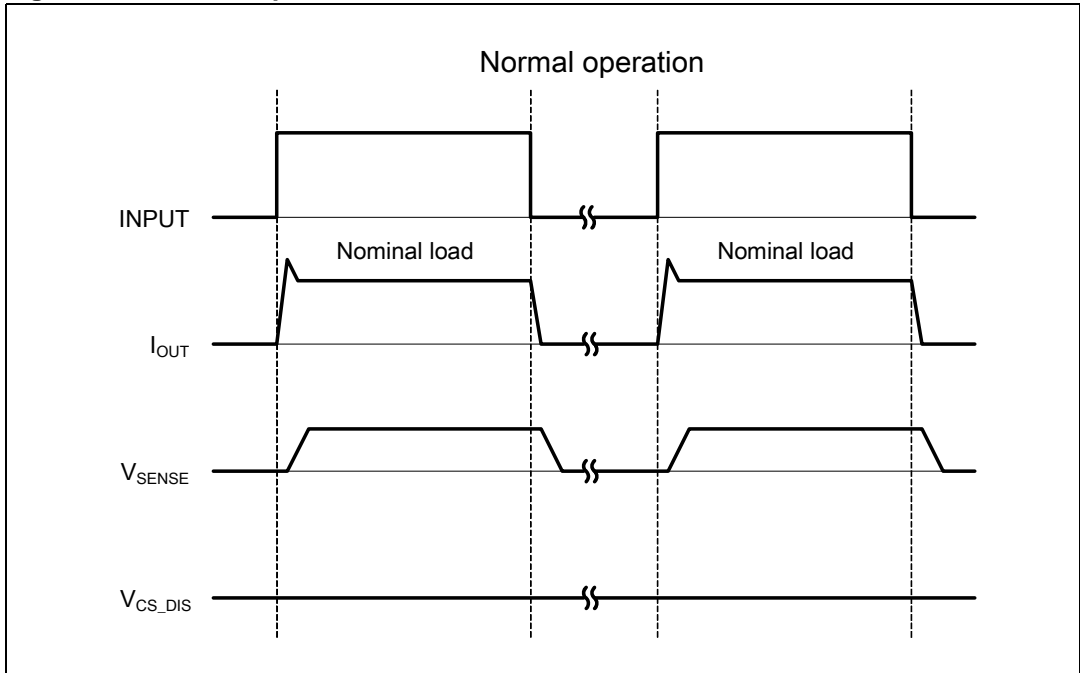


Figure 11. Overload or Short to GND

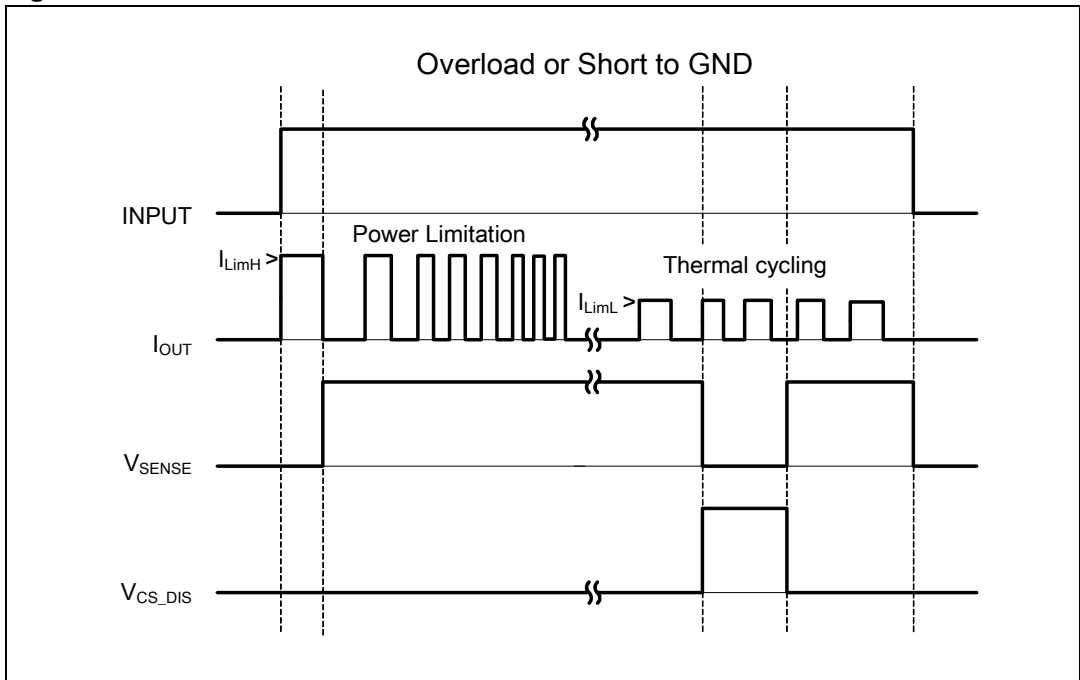


Figure 12. Intermittent Overload

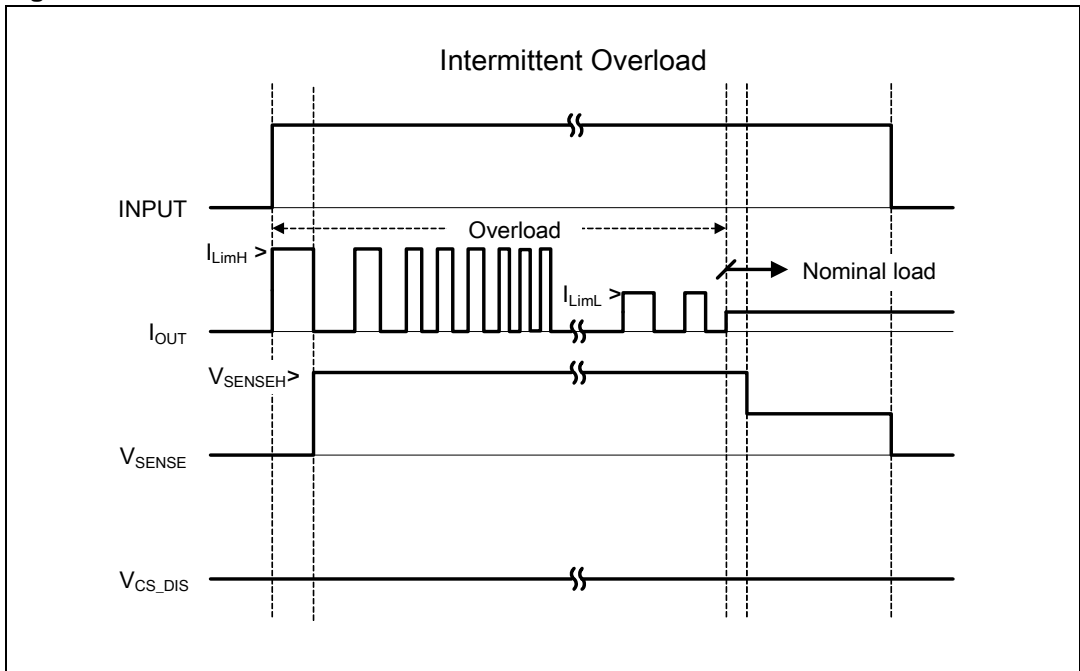
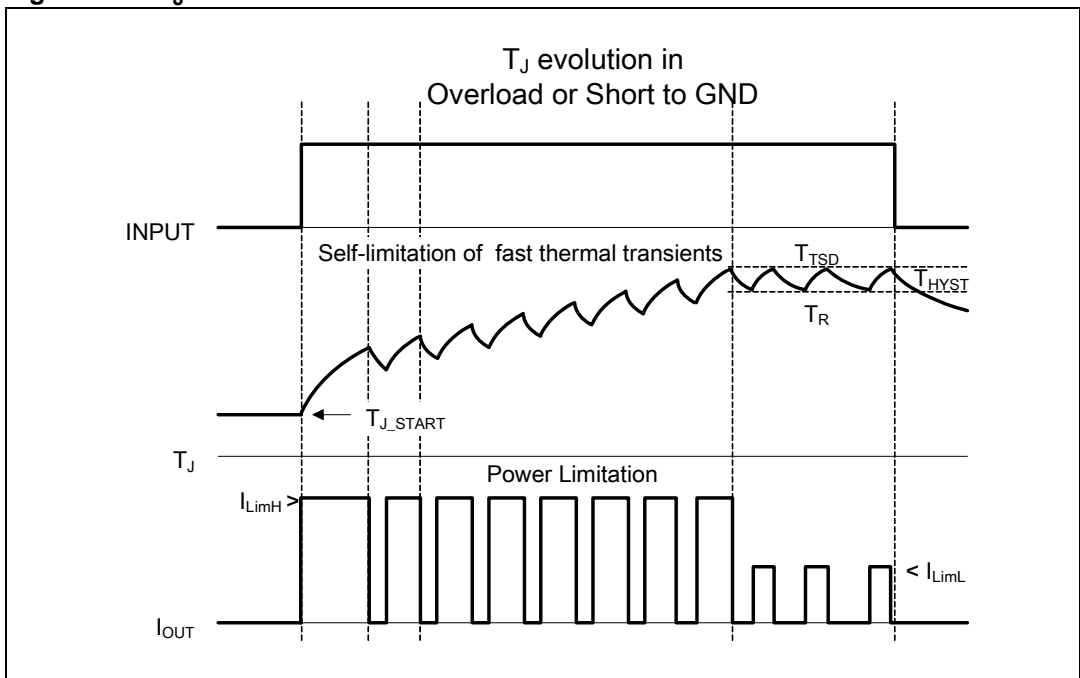


Figure 13. T_J evolution in Overload or Short to GND



2.5 Electrical characteristics curves

Figure 14. Off-state output current

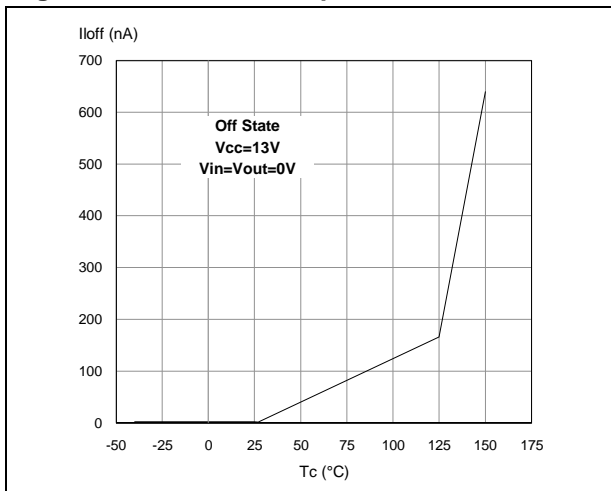


Figure 15. High level input current

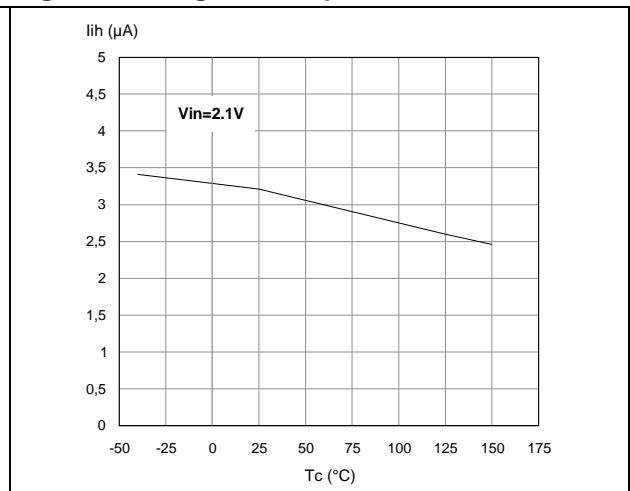


Figure 16. Input clamp level

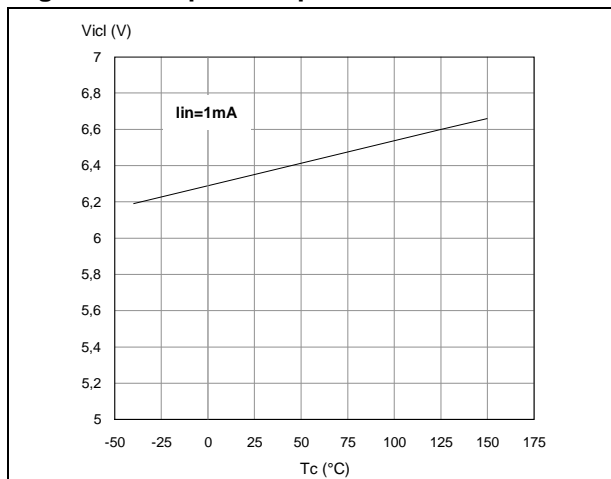


Figure 17. Input low level

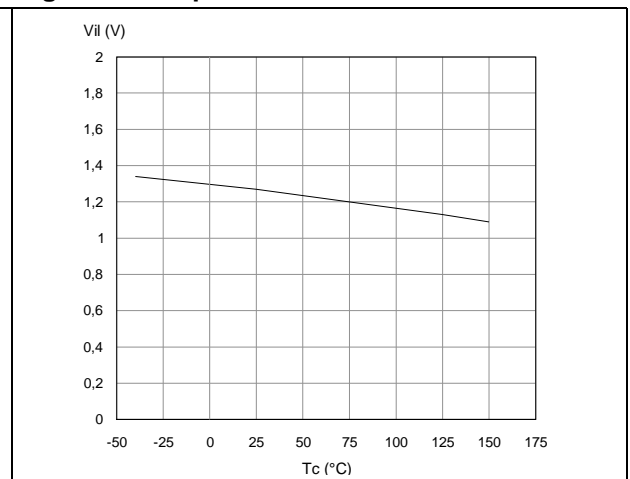


Figure 18. Input high level

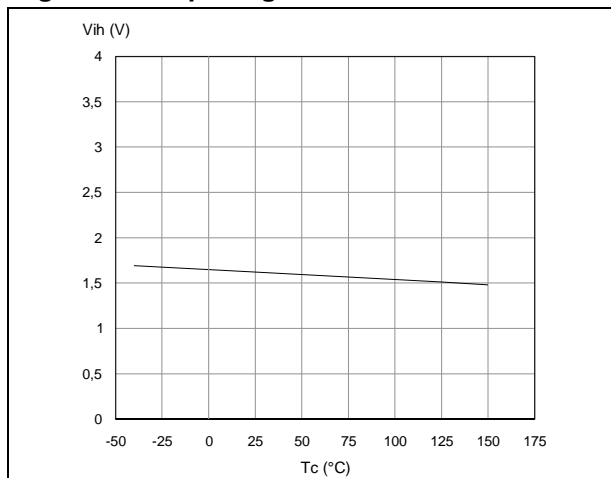


Figure 19. Input hysteresis voltage

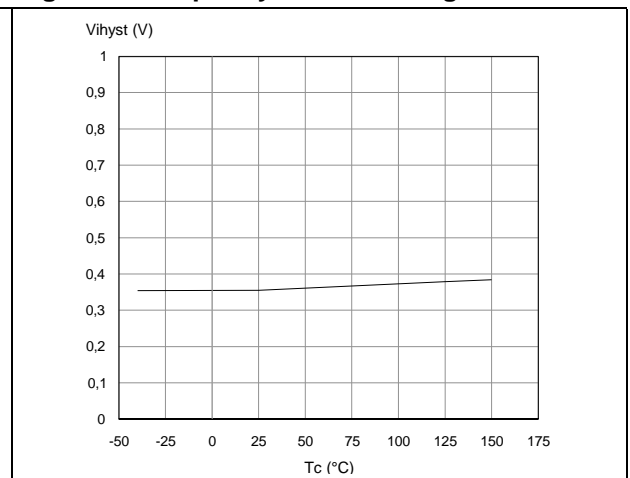


Figure 20. On-state resistance vs. T_{case}

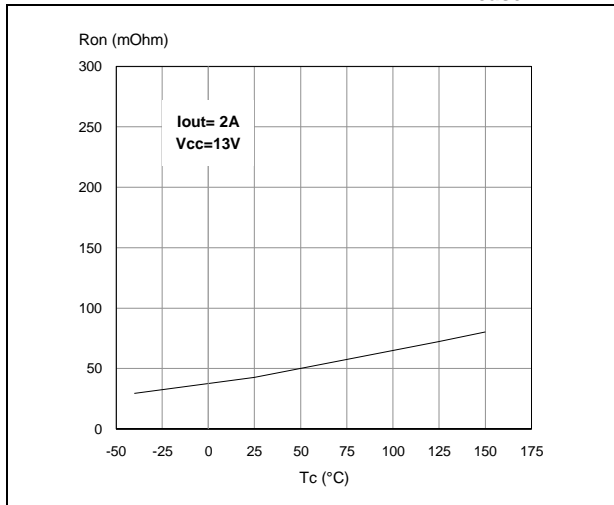


Figure 21. On-state resistance vs. V_{CC}

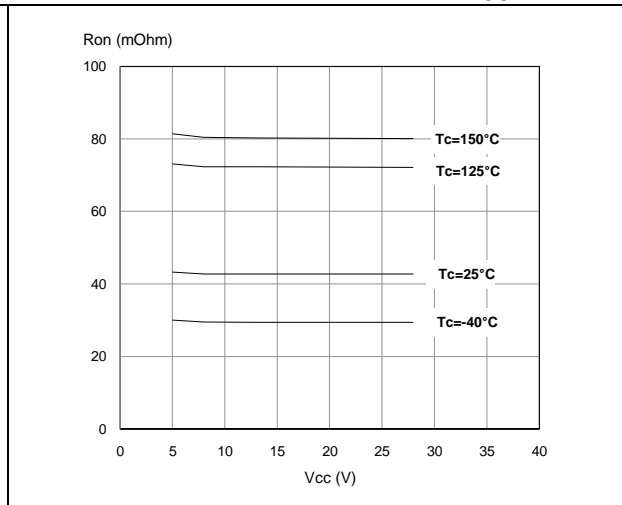


Figure 22. Undervoltage shutdown

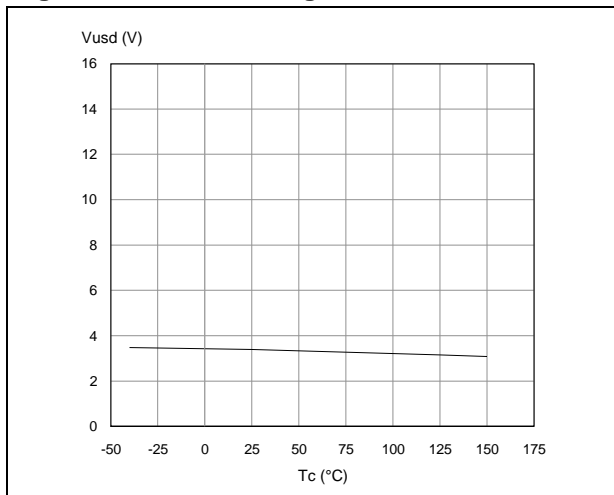


Figure 23. Turn-on voltage slope

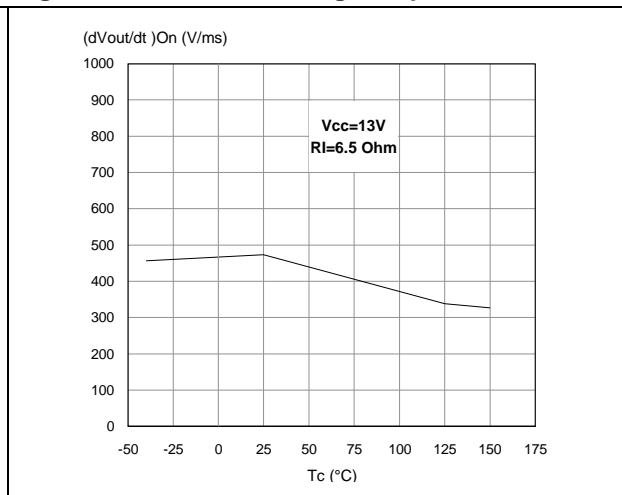


Figure 24. I_{LIMH} Vs. T_{case}

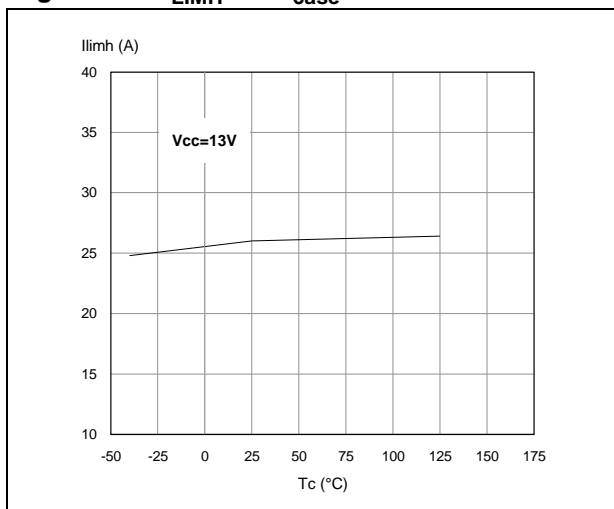


Figure 25. Turn-off voltage slope

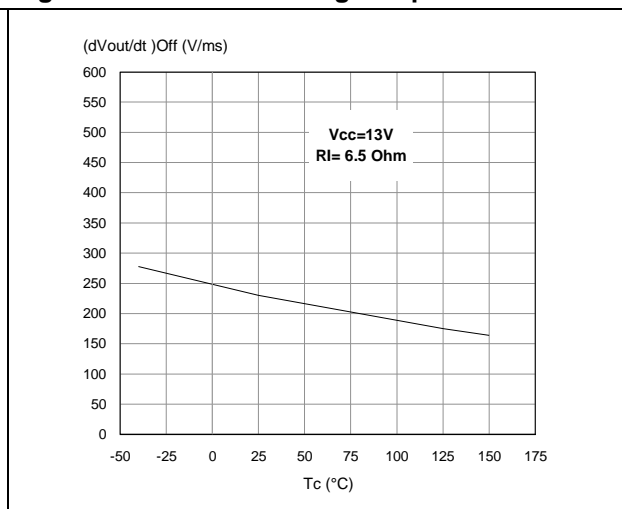


Figure 26. CS_DIS high level voltage

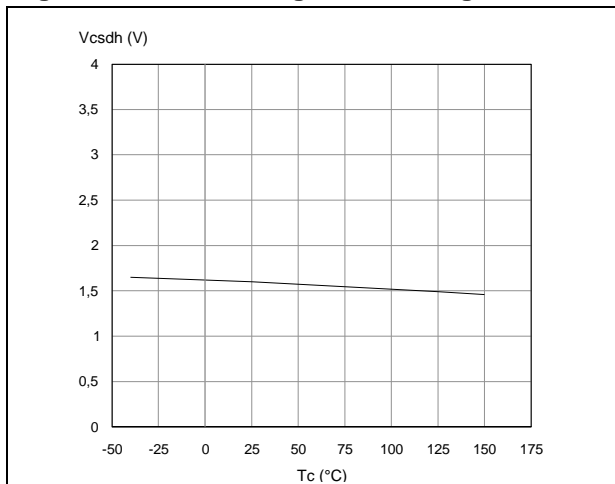


Figure 27. CS_DIS clamp voltage

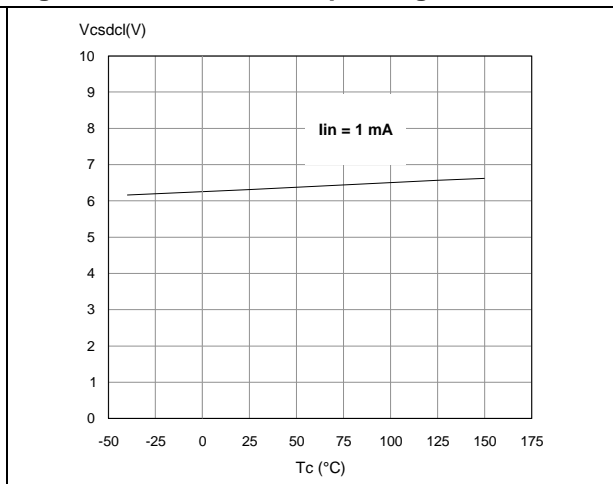
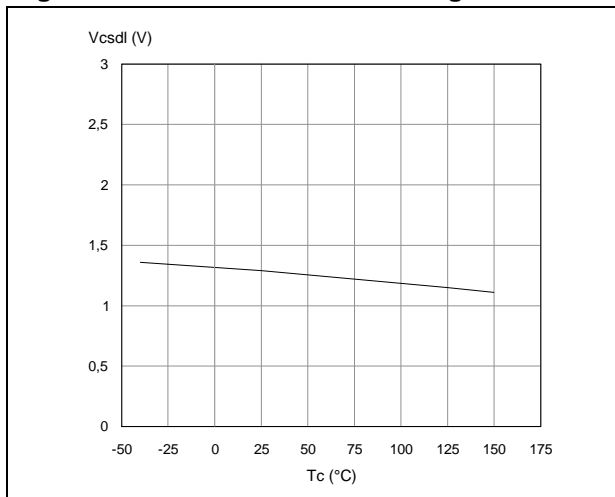
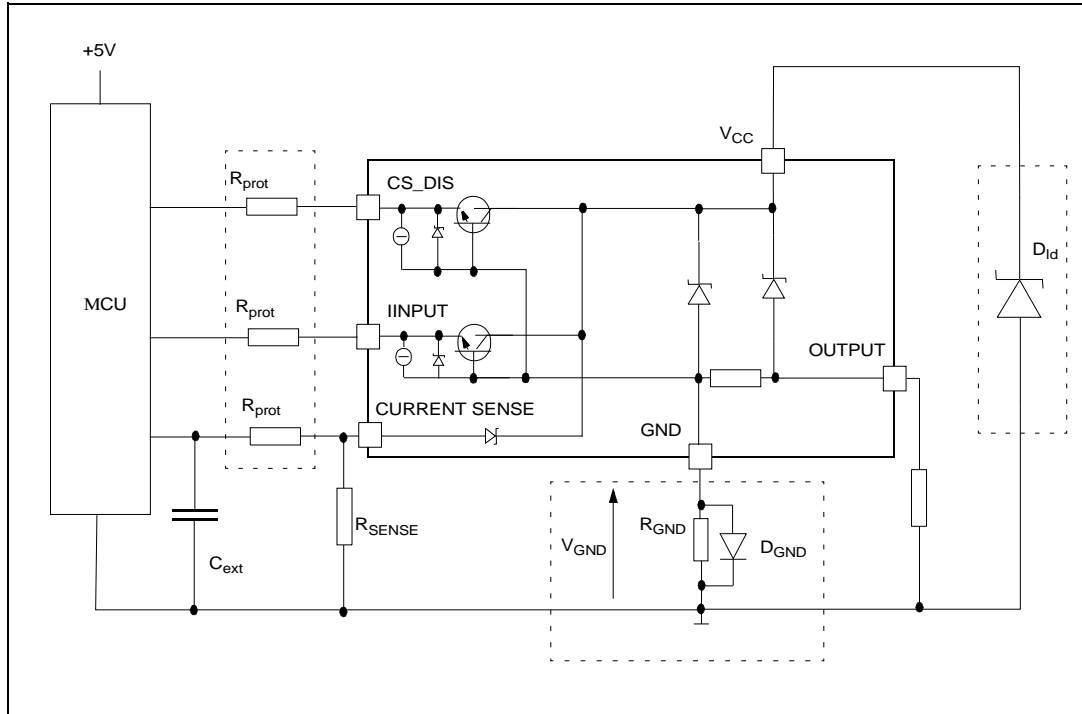


Figure 28. CS_DIS low level voltage



3 Application information

Figure 29. Application schematic



3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following show how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output

values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

3.1.2 Solution 2: diode (D_{GND}) in the ground line

Note that a resistor ($R_{GND}=1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (j600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift not varies if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins is pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the MCU I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of MCU and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of MCU I/Os:

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

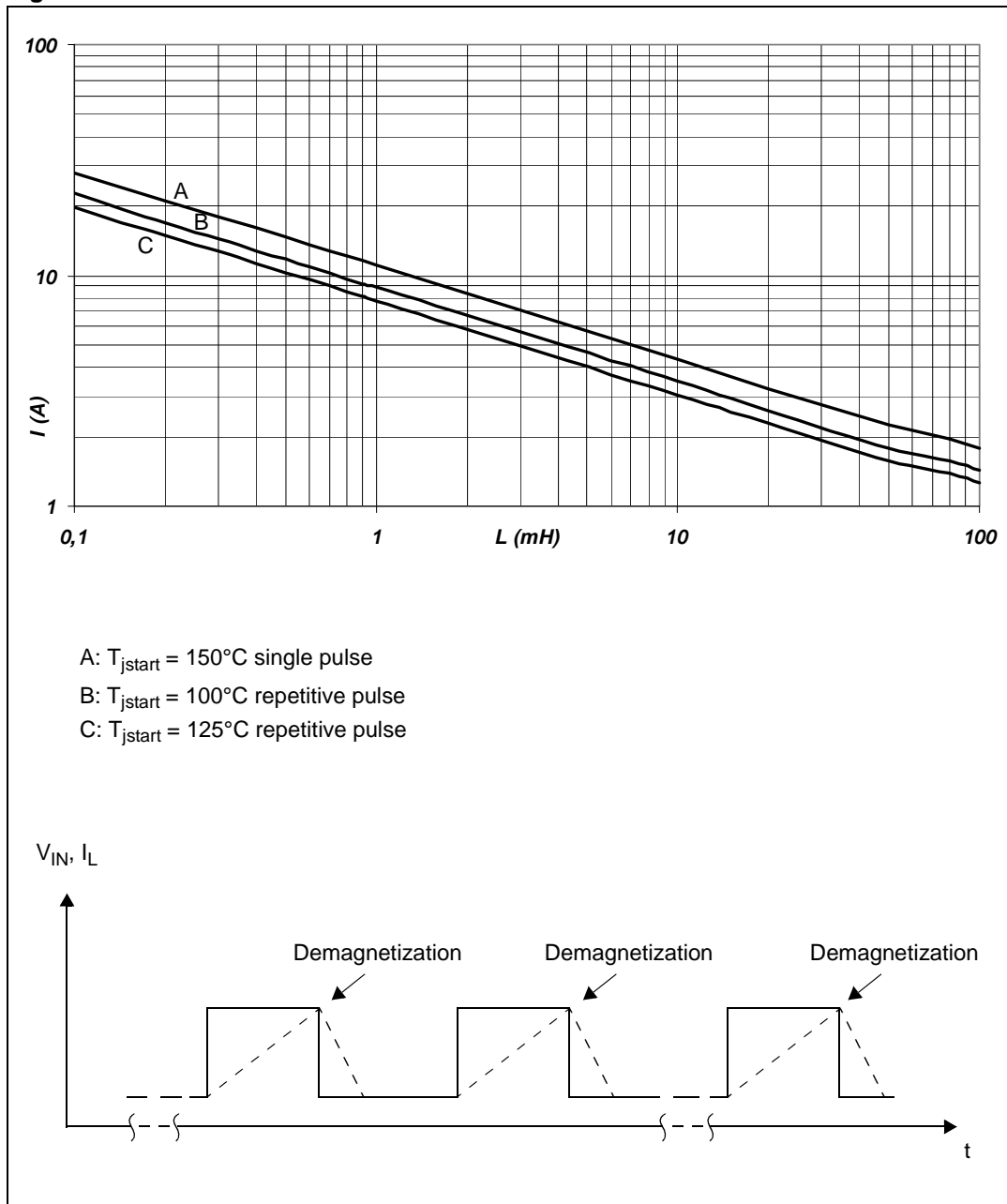
For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 180k\Omega$$

Recommended values: $R_{prot} = 10k\Omega$, $C_{EXT} = 10nF$.

3.5 Maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 31. Maximum turn-off current versus inductance

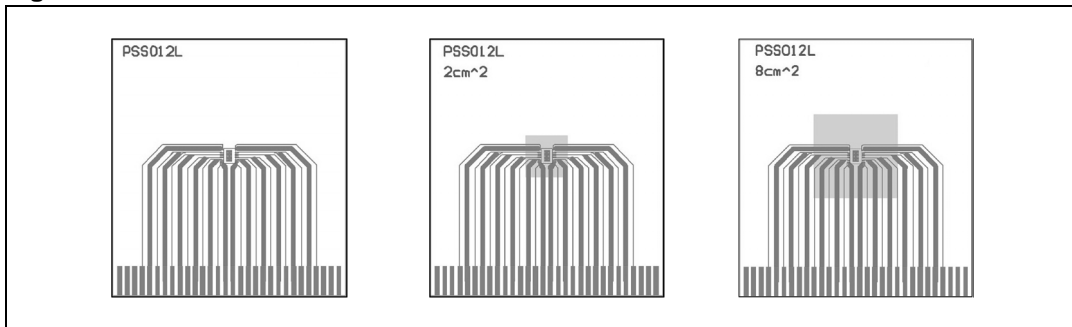


$L \Omega$. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-12 thermal data

Figure 32. PowerSSO-12 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 μ m (front and back side), Copper areas: from minimum pad lay-out to 8 cm²).

Figure 33. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

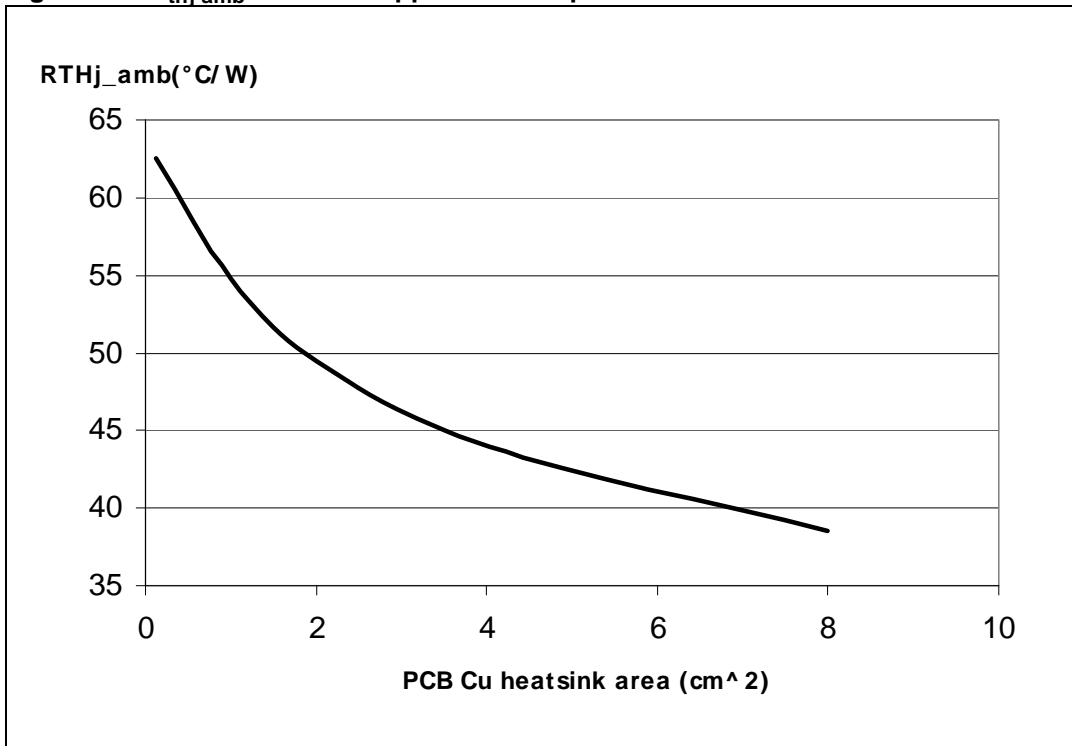
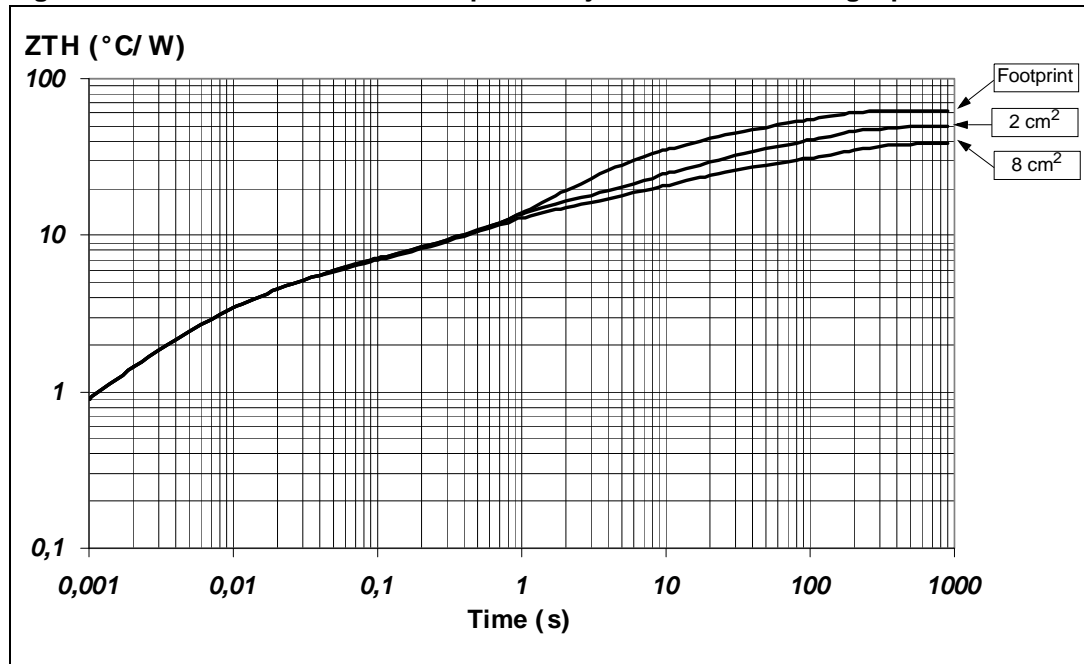


Figure 34. PowerSSO-12 thermal impedance junction ambient single pulse

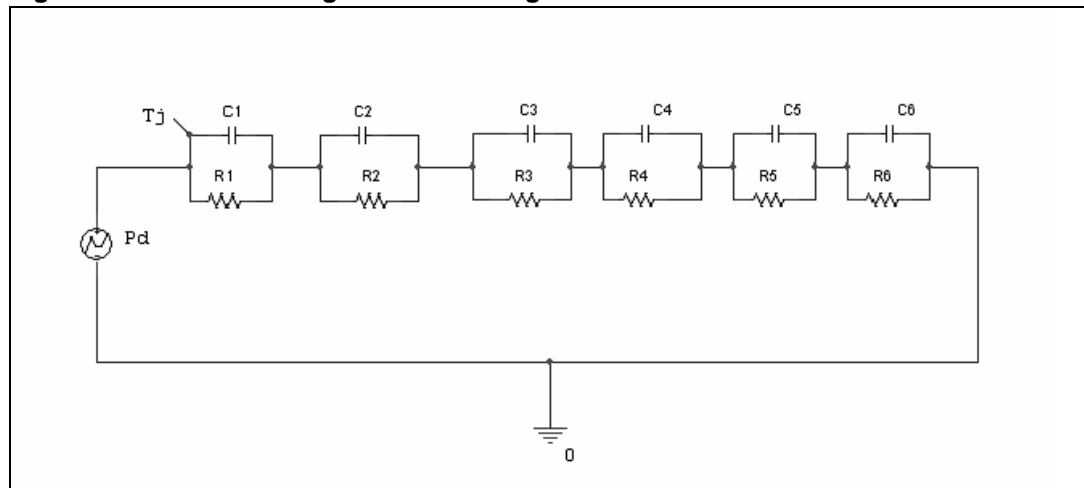


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 35. Thermal fitting model of a single channel HSD in PowerSSO-12 (a)



- a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 14. Thermal parameter

Area/island (cm ²)	Footprint	2	8
R1 (°C/W)	0.7		
R2 (°C/W)	2.8		
R3 (°C/W)	3		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.0025		
C3 (W.s/°C)	0.0166		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

5 Package information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 Package mechanical data

Figure 36. PowerSSO-12 package dimensions

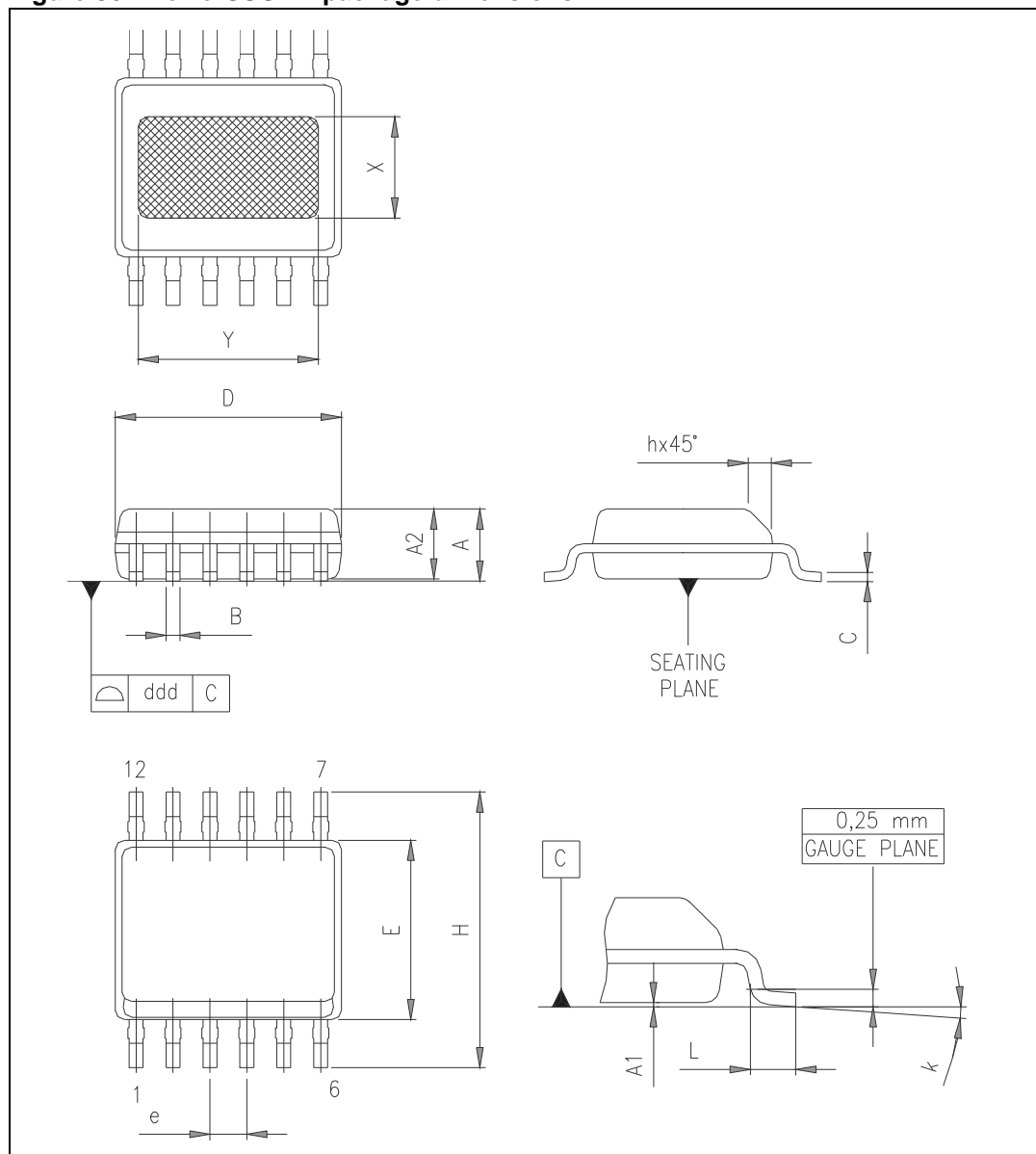


Table 15. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

5.3 Packing information

Figure 37. PowerSSO-12 tube shipment (no suffix)

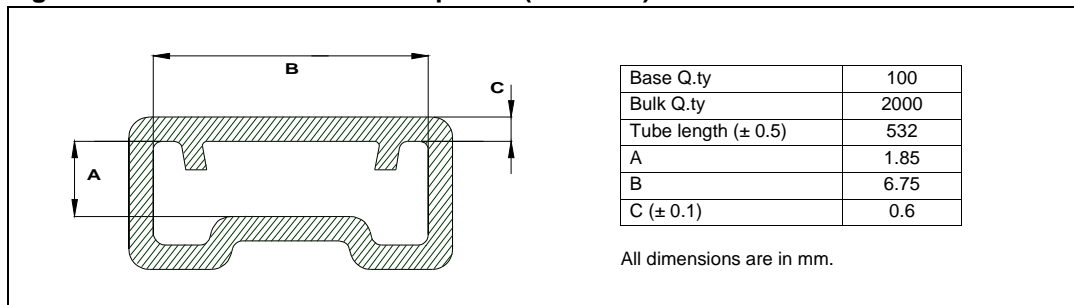
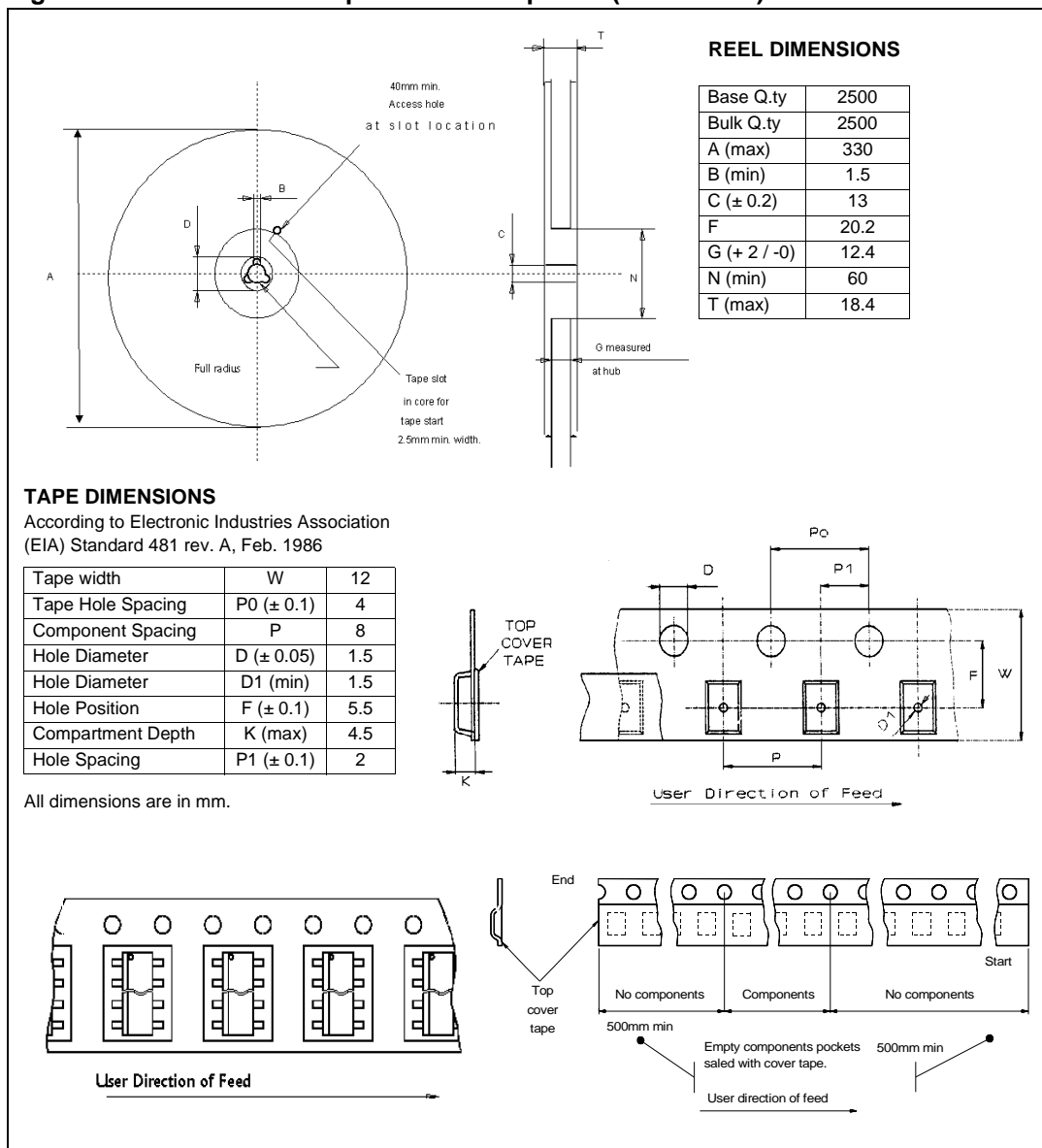


Figure 38. PowerSSO-12 tape and reel shipment (suffix “TR”)



6 Order codes

Table 16. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-12	VN5E050MJ-E	VN5E050MJTR-E

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
03-Nov-2009	1	Initial release.
19-Sep-2013	2	Updated Disclaimer.

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