TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOS VI)

SSM3J46CTB

Power Management Switch Applications

Unit: mm

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Low ON-resistance: RDS(ON) = 250 m Ω (max) (@VGS = -1.5 V)

 $RDS(ON) = 178 \text{ m}\Omega \text{ (max) (@VGS = -1.8 V)}$

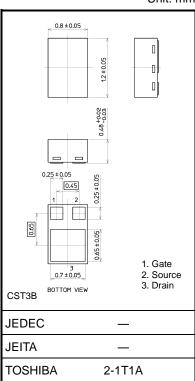
 $RDS(ON) = 133 \text{ m}\Omega \text{ (max) (@VGS = -2.5 V)}$

 $RDS(ON) = 103 \text{ m}\Omega \text{ (max) (@VGS = -4.5 V)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit	
Drain-Source voltage		VDSS	-20	V	
Gate-Source voltage		VGSS	± 8	V	
Drain current	DC	ID	-2.0	^	
Diain current	Pulse	IDP	-4.0	Α	
Power dissipation		P _D (Note 1)	1000	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature ra	ange	T _{stg}	−55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.



Weight: 1.5 mg (typ.)

Please design the appropriate reliability upon reviewing the

Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

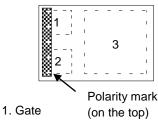
Note 1: Mounted on a FR4 board.

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 645 \text{ mm}^2)$

Marking (top view)

Polarity mark

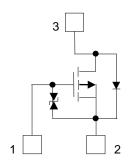
Pin Condition (top view)



- 2. Source
- 3. Drain

*Electrodes: on the bottom

Equivalent Circuit



Start of commercial production 2010-02

Electrical Characteristics (Ta = 25°C)

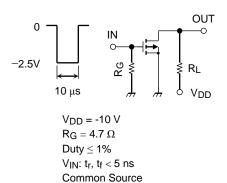
Characteristic		Symbol	Test Conditions		Min	Тур.	Max	Unit	
Drain-Source breakdown voltage		V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$		-20	_	_	V	
		V (BR) DSX	$I_D = -1$ mA, $V_{GS} = 5$ V	(Note 3)	-15	_	_	V	
Drain cut-off current		IDSS	V _{DS} = -20 V, V _{GS} = 0 V		_	_	-1	μΑ	
Gate leakage current		Igss	$VGS = \pm 8 \text{ V}, VDS = 0 \text{ V}$		_	_	±1	μΑ	
Gate threshold voltage		V _{th}	$V_{DS} = -3 \text{ V}, I_{D} = -1 \text{ mA}$		-0.3	_	-1.0	V	
Forward transfer admittance		Y _{fs}	$V_{DS} = -3 \text{ V}, I_{D} = -1.0 \text{ A}$	(Note 2)	_	5.2	_	S	
Drain-source ON-resistance			I _D = -1.5 A, V _G S = -4.5 V	(Note 2)	_	88.5	103	· mΩ	
		Pro (ov)	I _D = -1.0 A, V _G S = -2.5 V	(Note 2)	_	107.5	133		
		R _{DS} (ON)	$I_D = -0.5 \text{ A}, V_{GS} = -1.8 \text{ V}$	(Note 2)	_	130	178		
			$I_D = -0.25 \text{ A}, V_{GS} = -1.5 \text{ V}$	(Note 2)	_	151	250		
Input capacitance		Ciss	V 40.V.V 0.V		_	290	_		
Output capacitance		Coss	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}$ $f = 1 \text{ MHz}$		_	44	_	pF	
Reverse transfer capacitance		C _{rss}			_	32	_		
Switching time	Turn-on time	ton	$V_{DD} = -10 \text{ V}, I_D = -0.5 \text{ A}$	Σ	_	13.4	_	ns	
	Turn-off time	t _{off}	$V_{GS} = 0$ to -2.5 V, $R_{G} = 4.7$ Ω		_	46.2	_		
Total Gate Charge		Qg	\/ 40\/ I- 00A		_	4.7	_		
Gate-Source Charge		Q _{gs1}	$V_{DD} = -10 \text{ V}, \text{ ID} = -2.0 \text{ A},$ $V_{GS} = -4.5 \text{ V}$		_	0.4	_	nC	
Gate-Drain Charge		Q _{gd}	v GS = - 4.5 v		_	1.0	_		
Drain-Source forward voltage		V _{DSF}	I _D = 2.0 A, V _{GS} = 0 V	(Note 2)	_	0.9	1.2	V	

Note2: Pulse test

Note3: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

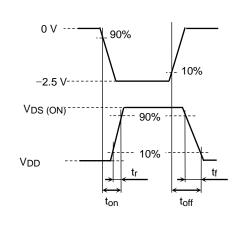
Switching Time Test Circuit





(b) VIN

(c) Vout



Notice on Usage

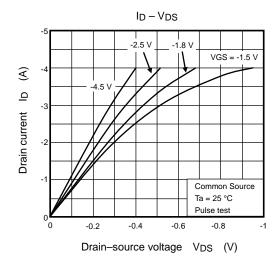
 $Ta = 25^{\circ}C$

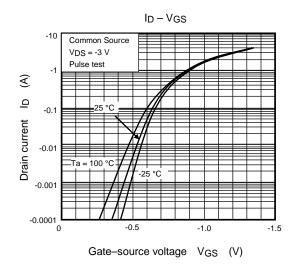
Vth can be expressed as the voltage between gate and source when the low operating current value is ID = -1 mA for this product. For normal switching operation, VGS (on) requires a higher voltage than Vth and VGS (off) requires a lower voltage than Vth. (The relationship can be established as follows: VGS (off) < Vth < VGS (on).)

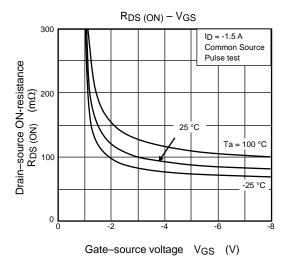
Take this into consideration when using the device.

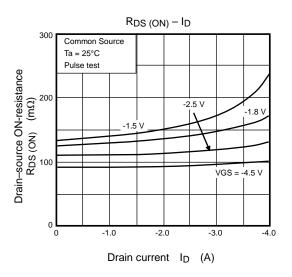
Handling Precaution

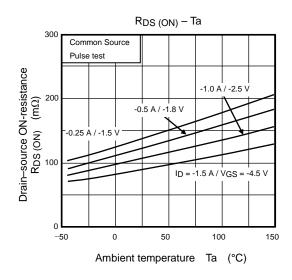
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

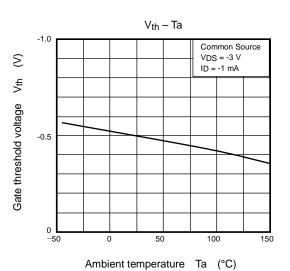




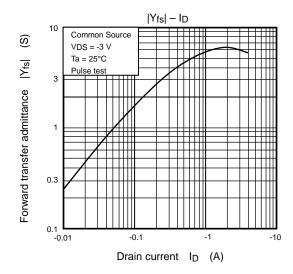


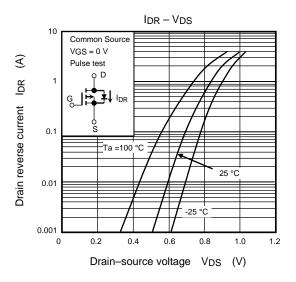


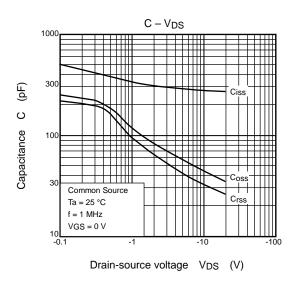


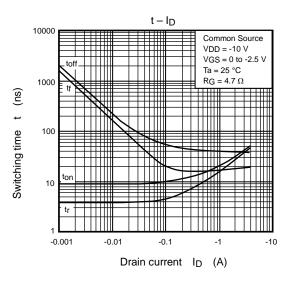


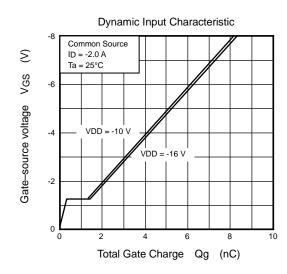
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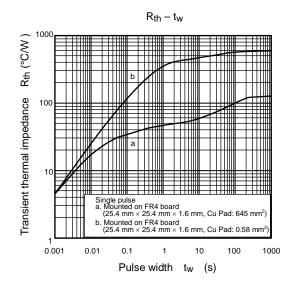


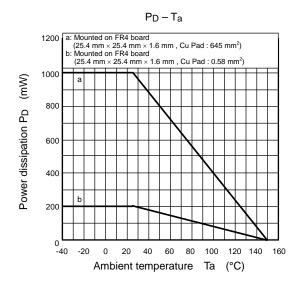












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