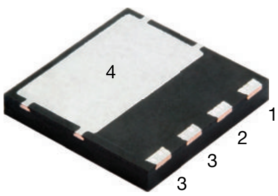
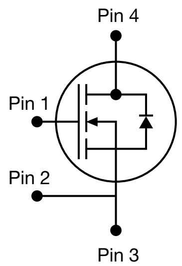
E Series Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ typ. (Ω) at 25 °C	V_{GS} = 10 V	0.148
Q_g max. (nC)	99	
Q_{gs} (nC)	16	
Q_{gd} (nC)	28	
Configuration	Single	

PowerPAK® 8 x 8





N-Channel MOSFET

FEATURES

- Completely lead (Pb)-free device
- Low figure-of-merit (FOM) R_{on} x Q_g
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Kelvin connection for reduced gate noise
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

ORDERING INFORMATION	
Package	PowerPAK 8 x 8
Lead (Pb)-free and Halogen-free	SiHH21N65E-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

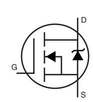
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	650	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	20.3	A
		T_C = 100 °C		12.8	
Pulsed Drain Current [a]			I_{DM}	53	
Linear Derating Factor				1.47	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	353	mJ
Maximum Power Dissipation			P_D	156	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	70	V/ns
Reverse Diode dV/dt [c]				17	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 5 A.
c. $I_{SD} \leq I_D$, dI/dt = 100 A/μs, starting T_J = 25 °C.

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	39	51	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	0.51	0.68	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.81	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
		V_{GS} = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V		-	-	1	μA
		V_{DS} = 520 V, V_{GS} = 0 V, T_J = 125 °C		-	-	25	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 11 A	-	0.148	0.170	Ω
Forward Transconductance	g_{fs}	V_{DS} = 30 V, I_D = 11 A		-	8.5	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz		-	2404	-	pF
Output Capacitance	C_{oss}			-	102	-	
Reverse Transfer Capacitance	C_{rss}			-	2	-	
Effective Output Capacitance, Energy Related [a]	$C_{o(er)}$	V_{DS} = 0 V to 520 V, V_{GS} = 0 V		-	75	-	
Effective Output Capacitance, Time Related [b]	$C_{o(tr)}$			-	314	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 11 A, V_{DS} = 520 V	-	66	99	nC
Gate-Source Charge	Q_{gs}			-	16	-	
Gate-Drain Charge	Q_{gd}			-	28	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 520 V, I_D = 11 A, V_{GS} = 10 V, R_g = 9.1 Ω		-	26	52	ns
Rise Time	t_r			-	46	92	
Turn-Off Delay Time	$t_{d(off)}$			-	69	104	
Fall Time	t_f			-	44	88	
Gate Input Resistance	R_g	f = 1 MHz, open drain		0.27	0.55	1.10	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	20.3	A
Pulsed Diode Forward Current	I_{SM}			-	-	53	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 11 A, V_{GS} = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 11 A, dI/dt = 100 A/μs, V_R = 25 V		-	396	792	ns
Reverse Recovery Charge	Q_{rr}			-	6.2	12.4	μC
Reverse Recovery Current	I_{RRM}			-	26	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT
ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

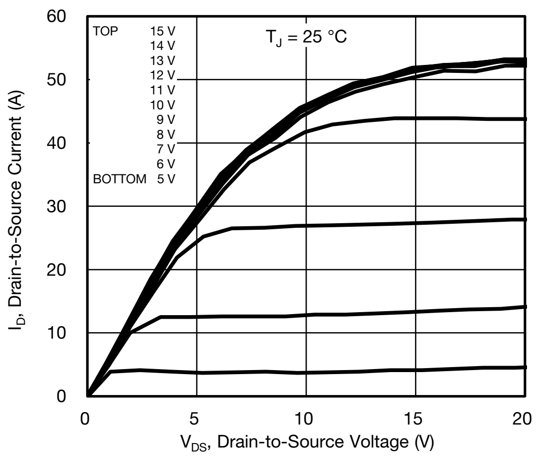


Fig. 1 - Typical Output Characteristics

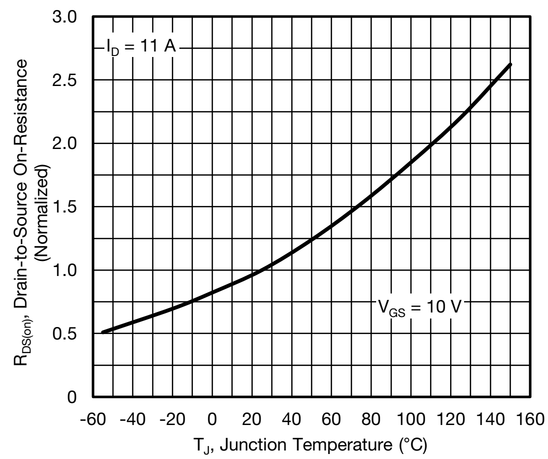


Fig. 4 - Normalized On-Resistance vs. Temperature

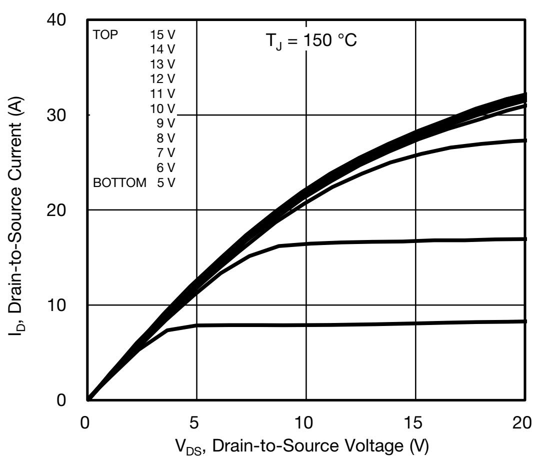


Fig. 2 - Typical Output Characteristics

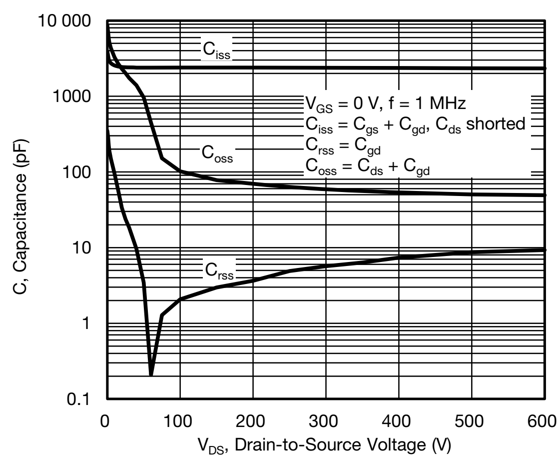


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

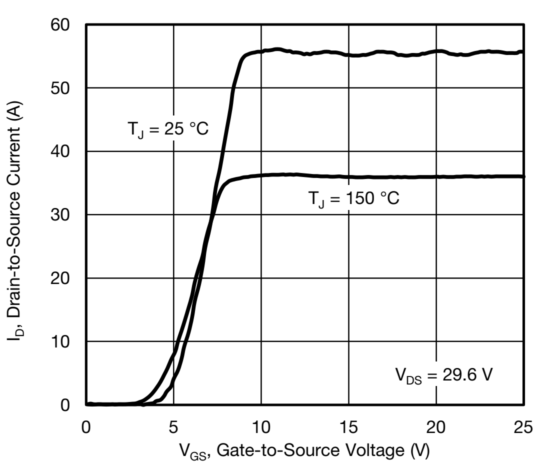


Fig. 3 - Typical Transfer Characteristics

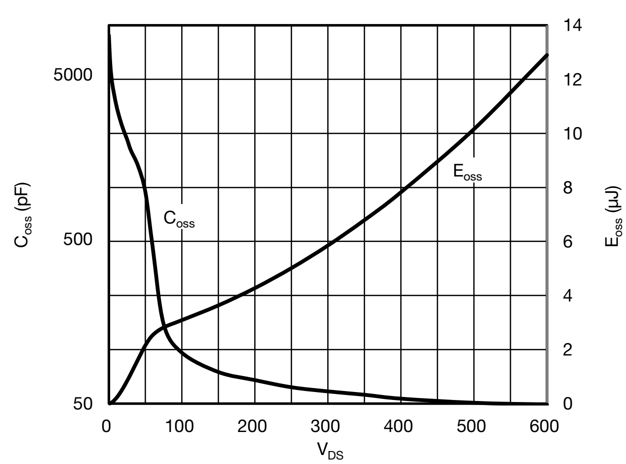


Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}

For technical questions, contact: hvm@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

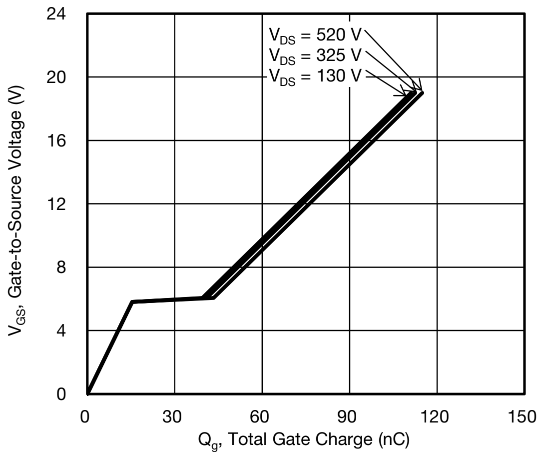


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

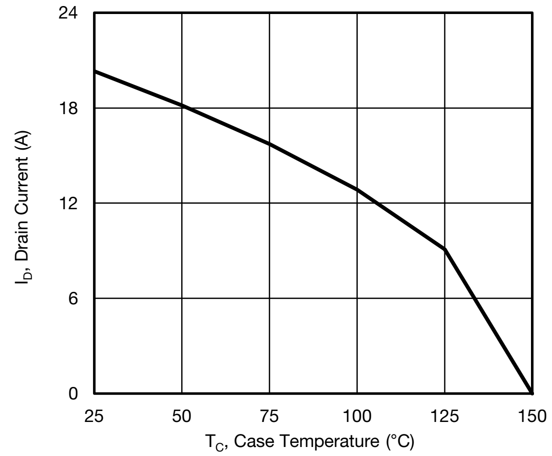


Fig. 10 - Maximum Drain Current vs. Case Temperature

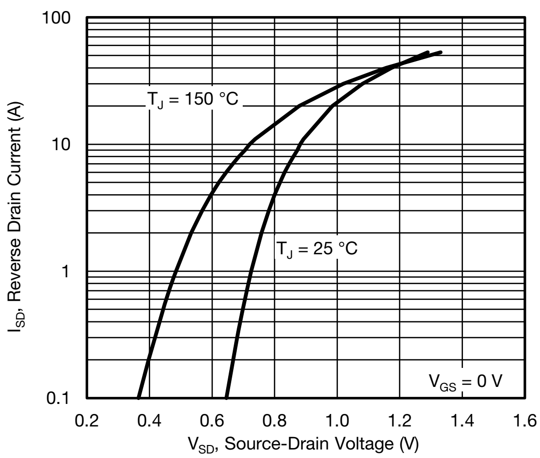


Fig. 8 - Typical Source-Drain Diode Forward Voltage

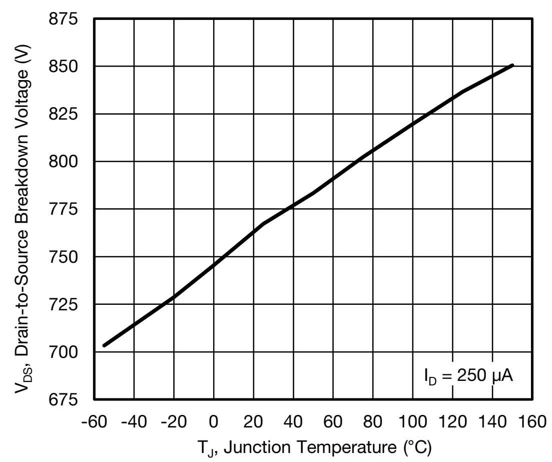
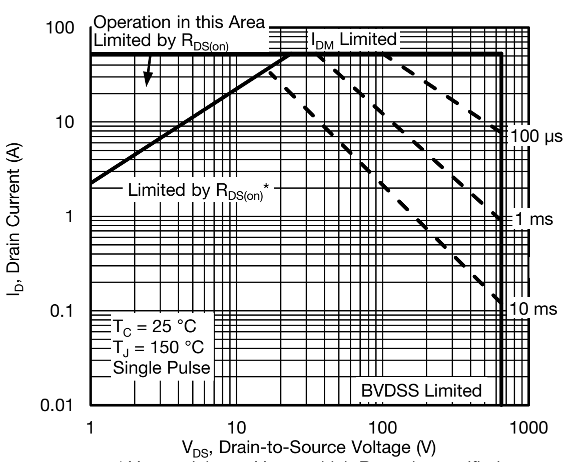


Fig. 11 - Temperature vs. Drain-to-Source Voltage



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Fig. 9 - Maximum Safe Operating Area

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

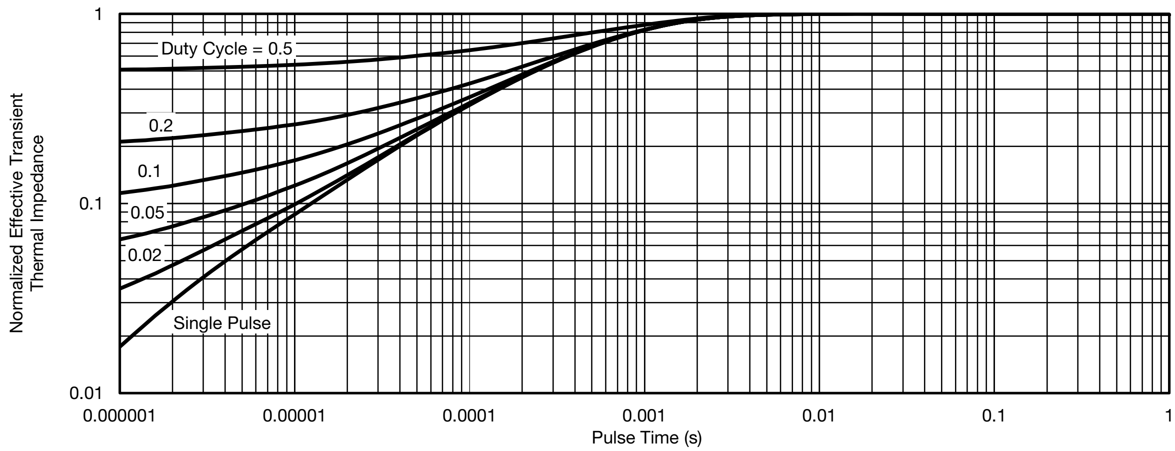


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

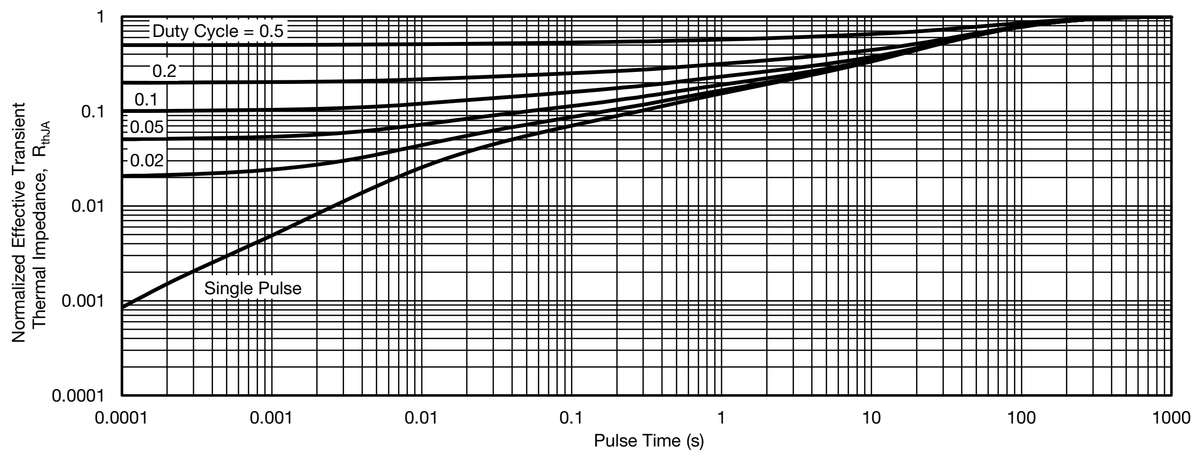


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

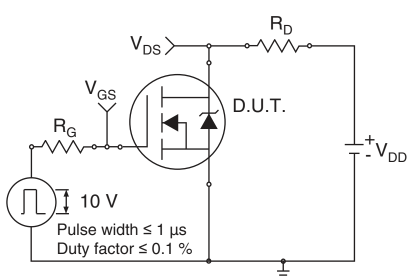


Fig. 14 - Switching Time Test Circuit

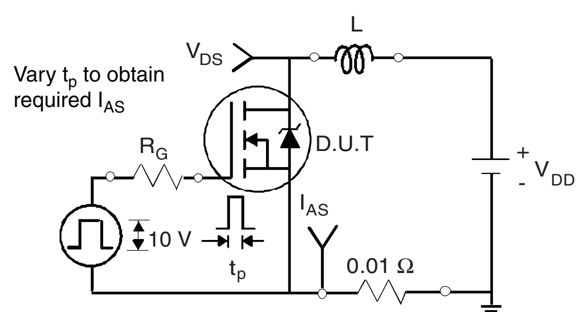


Fig. 16 - Unclamped Inductive Test Circuit

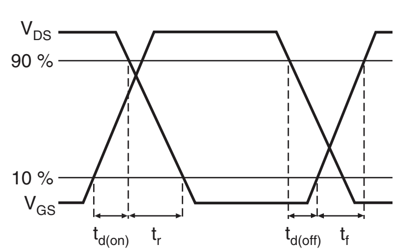


Fig. 15 - Switching Time Waveforms

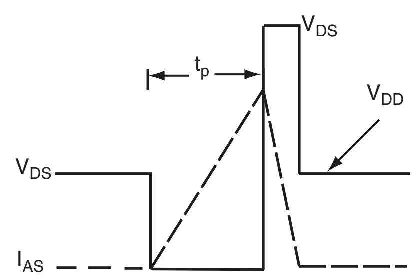


Fig. 17 - Unclamped Inductive Waveforms

For technical questions, contact: hvm@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

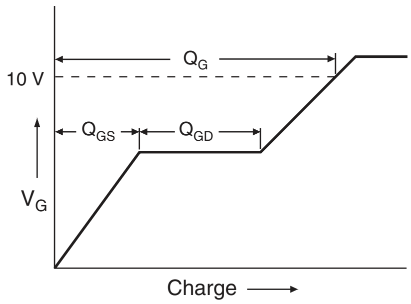


Fig. 18 - Basic Gate Charge Waveform

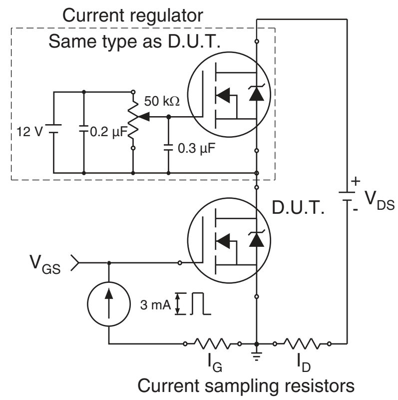
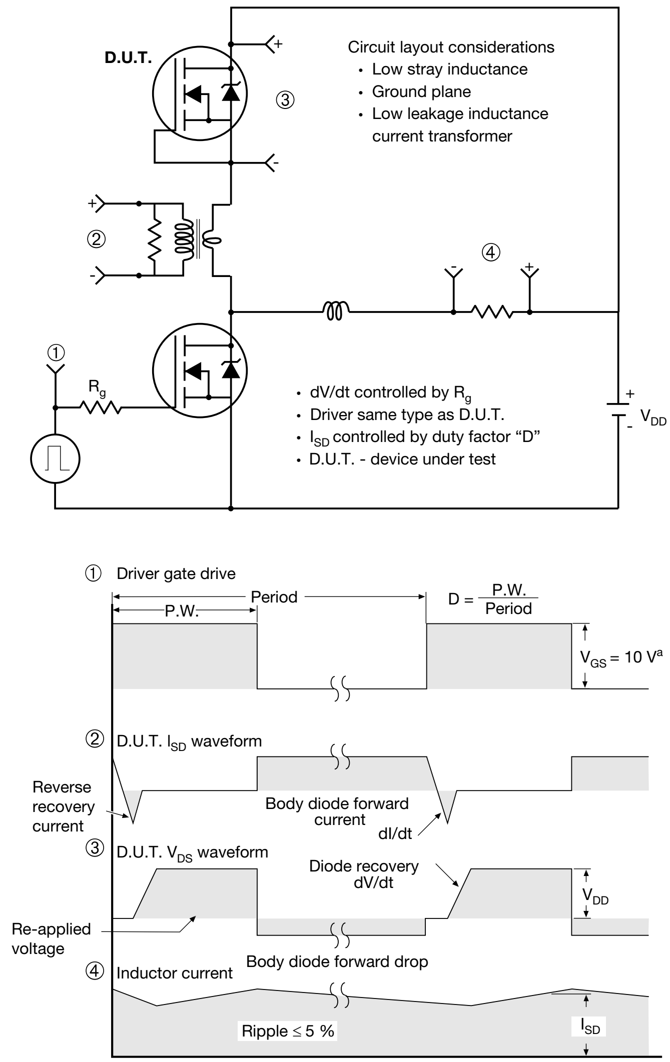


Fig. 19 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

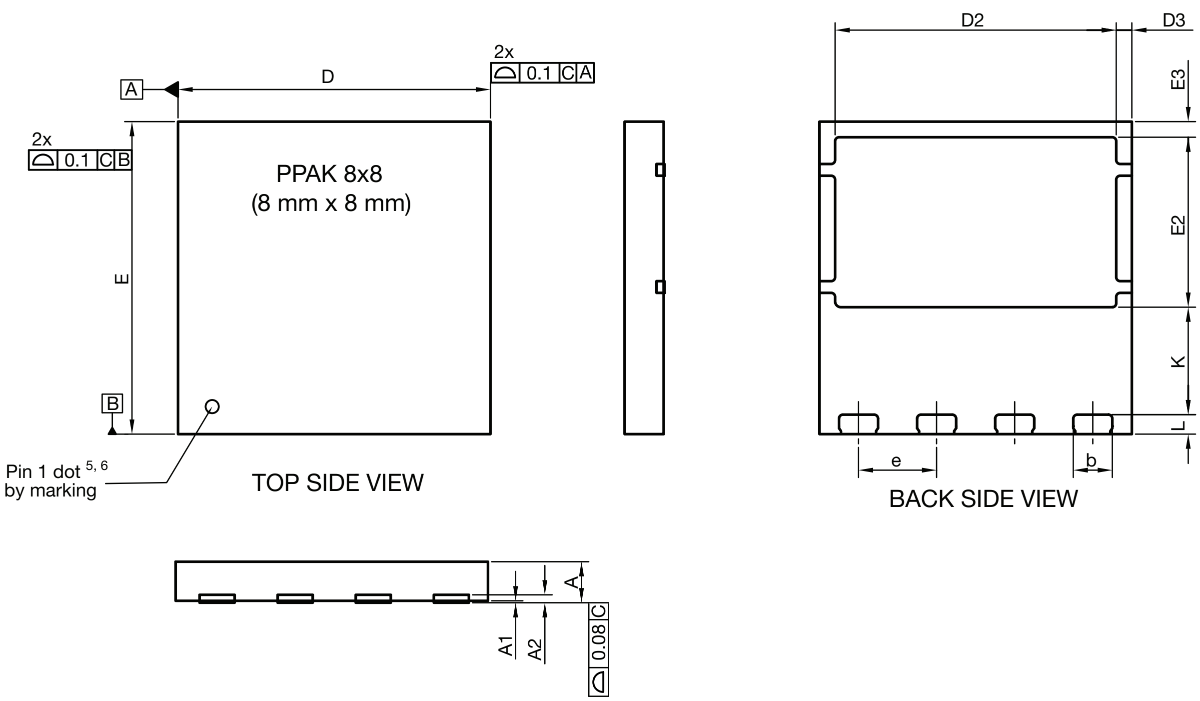
a. V_{GS} = 5 V for logic level devices

Fig. 20 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91738.

For technical questions, contact: hvm@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

PowerPAK® 8 x 8 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A [8]	0.95	1.00	1.05	0.037	0.039	0.041
A1	0.00	-	0.05	0.000	-	0.002
A2	020 ref.			0.008 ref.		
b [4]	0.95	1.00	1.05	0.037	0.039	0.041
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	7.10	7.20	7.30	0.280	0.283	0.287
D3	0.40 BSC			0.016 BSC		
e	2.00 BSC			0.079 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E2	4.30	4.35	4.40	0.169	0.171	0.173
E3	0.40 BSC			0.016 BSC		
K	2.75 BSC			0.108 BSC		
L	0.45	0.50	0.55	0.018	0.020	0.022
N [3]	8			8		

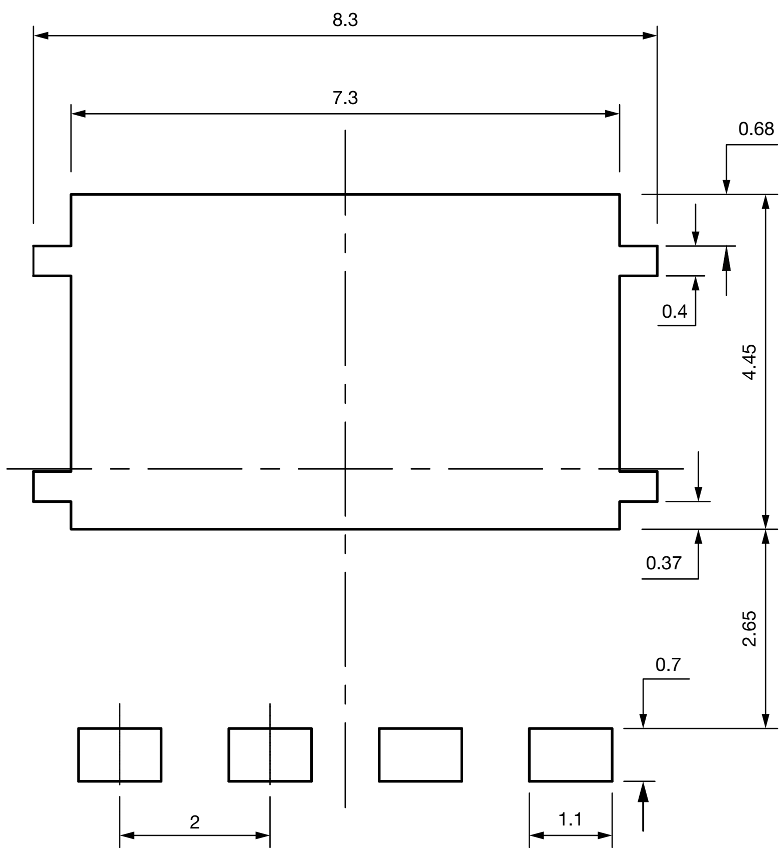
Notes

1. Use millimeters as the primary measurement.
2. Dimensioning and tolerances conform to ASME Y14.5 M - 1994.
3. N is the number of terminals.
4. Package warpage max. 0.08 mm.
5. The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.

ECN: T15-0225-Rev. A, 18-May-15
DWG: 6041

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

Recommended Minimum PADs for PowerPAK® 8 mm x 8 mm



Dimensions in millimeters

For technical questions, contact: pmostechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay’s knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer’s responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer’s technical experts. Product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Vishay:

SiHH21N65E-T1-GE3