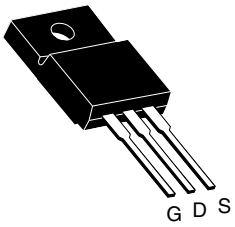
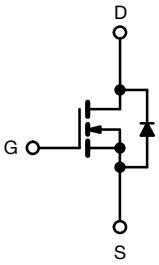
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	560	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	1
Q_g max. (nC)	34	
Q_{gs} (nC)	7.8	
Q_{gd} (nC)	10.4	
Configuration	Single	

TO-220 FULLPAK





N-Channel MOSFET

FEATURES

- Low figure-of-merit R_{on} x Q_g
- 100 % avalanche tested
- Gate charge improved
- t_{rr}/Q_{rr} improved
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF8N50L-E3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current [a]	V_{GS} at 10 V	T_C = 25 °C	I_D	8	A
Pulsed Drain Current [b]			I_{DM}	22	
Linear Derating Factor				0.32	W/°C
Single Pulse Avalanche Energy [c]			E_{AS}	180	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	40	W
Peak Diode Recovery dV/dt [d]			dV/dt	24	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) [e]	for 10 s			300	

Notes

a. Drain current limited by maximum junction temperature.
b. Repetitive rating; pulse width limited by maximum junction temperature.
c. V_{DD} = 50 V, starting T_J = 25 °C, L = 10 mH, R_g = 25 Ω, I_{AS} = 6 A.
d. $I_{SD} \leq$ 8 A, dI/dt $\leq$ 460 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
e. 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.5	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V		-	-	50	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 4.0 A	-	0.85	1	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3 A		-	2	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz		-	873	-	pF
Output Capacitance	C_{oss}			-	105	-	
Reverse Transfer Capacitance	C_{rss}			-	11	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 6 A, V_{DS} = 400 V	-	22	34	nC
Gate-Source Charge	Q_{gs}			-	7.8	-	
Gate-Drain Charge	Q_{gd}			-	10.4	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 6 A R_G = 14 Ω, V_{GS} = 10 V		-	17.3	-	ns
Rise Time	t_r			-	35	-	
Turn-Off Delay Time	$t_{d(off)}$			-	23.6	-	
Fall Time	t_f			-	17	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain		-	0.7	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	8	A
Pulsed Diode Forward Current	I_{SM}			-	-	22	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 8 A, V_{GS} = 0 V		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S, dI/dt = 100 A/μs, V_R = 15 V		-	63	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	114	-	nC
Body Diode Reverse Recovery Current	I_{RRM}			-	3.3	-	A

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

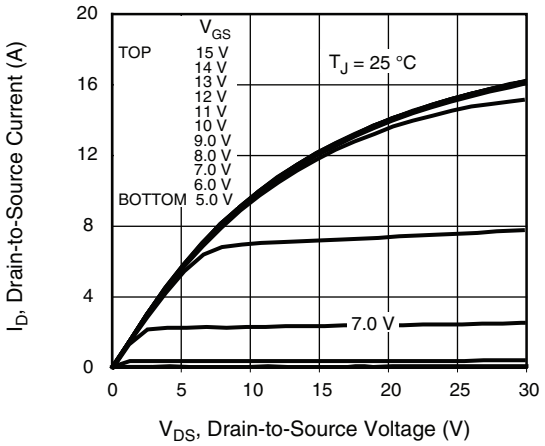


Fig. 1 - Typical Output Characteristics

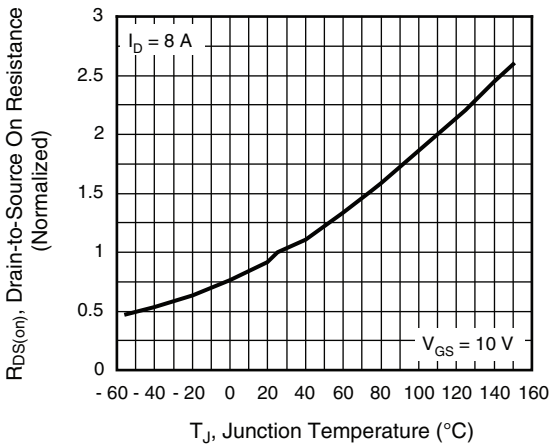


Fig. 4 - Normalized On-Resistance vs. Temperature

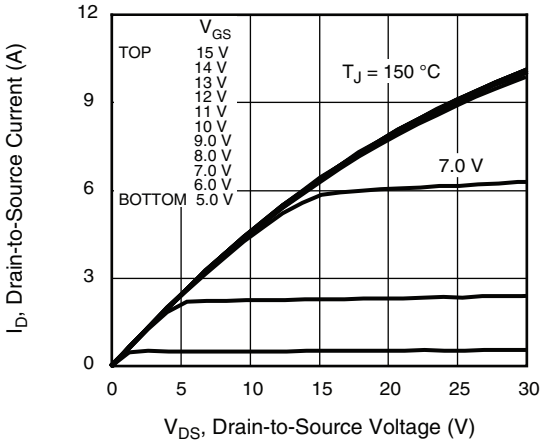


Fig. 2 - Typical Output Characteristics

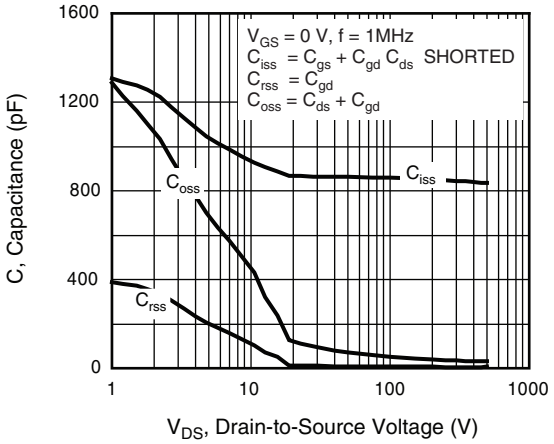


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

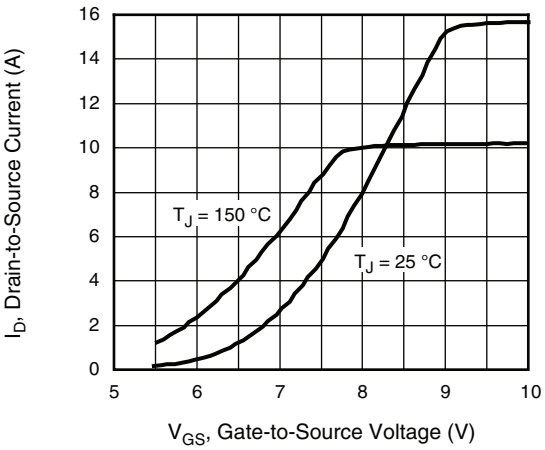


Fig. 3 - Typical Transfer Characteristics

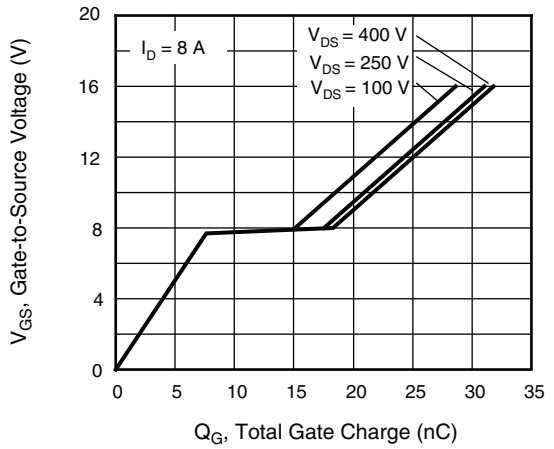


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

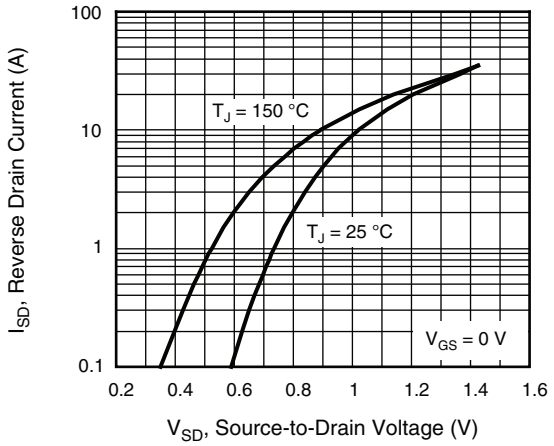


Fig. 7 - Typical Source-Drain Diode Forward Voltage

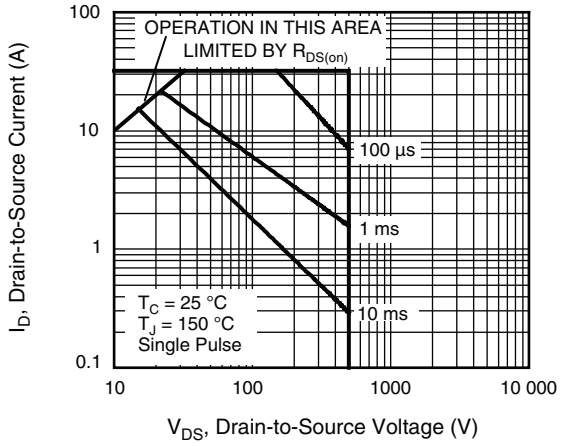


Fig. 8 - Maximum Safe Operating Area

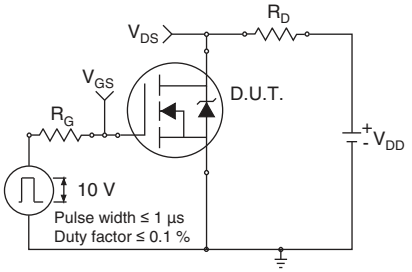


Fig. 9a - Switching Time Test Circuit

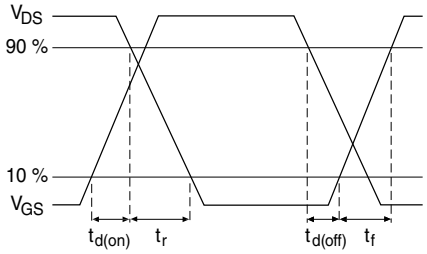


Fig. 9b - Switching Time Waveforms

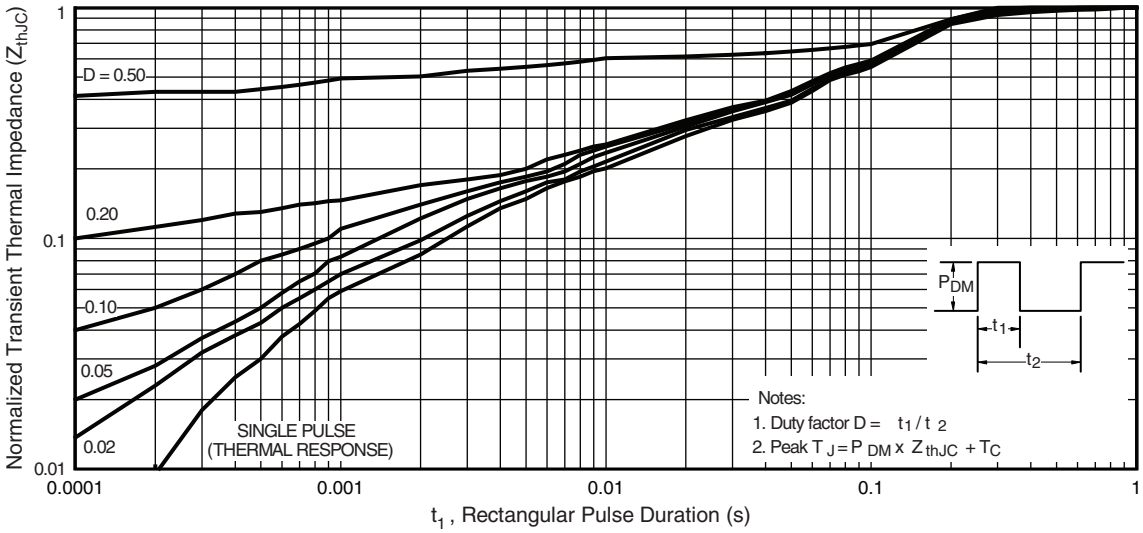


Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

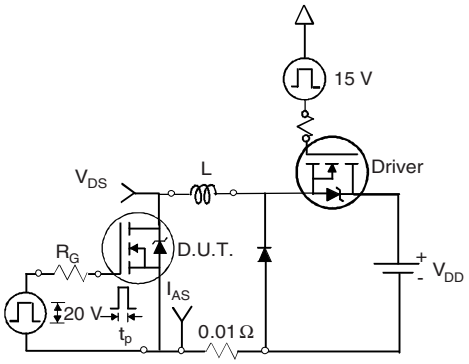


Fig. 11a - Unclamped Inductive Test Circuit

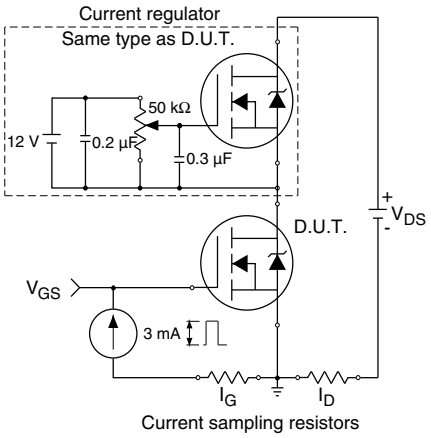


Fig. 12b - Gate Charge Test Circuit

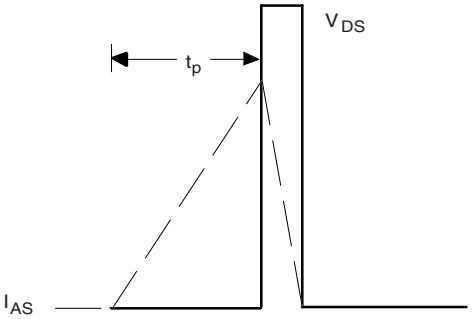


Fig. 11b - Unclamped Inductive Waveforms

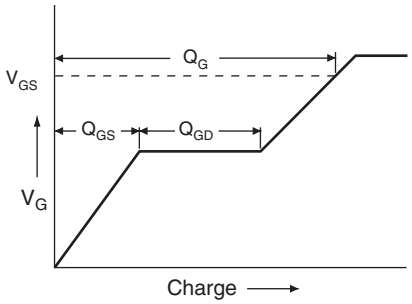
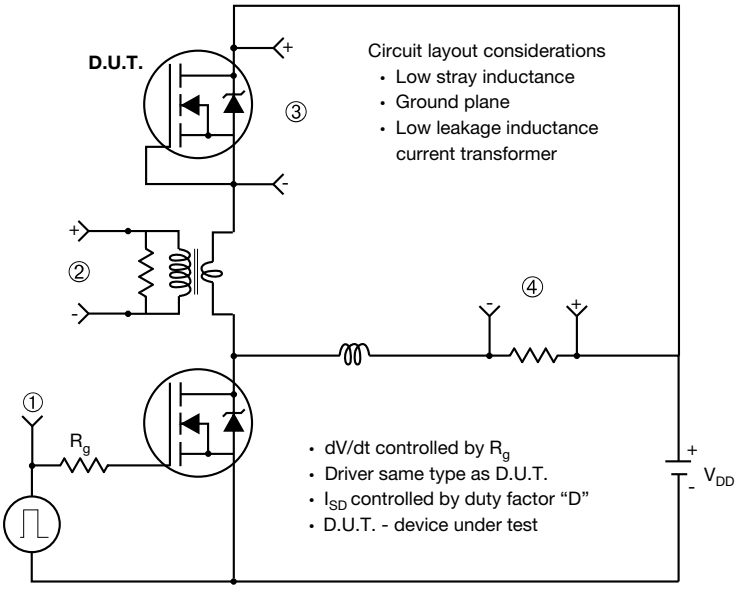
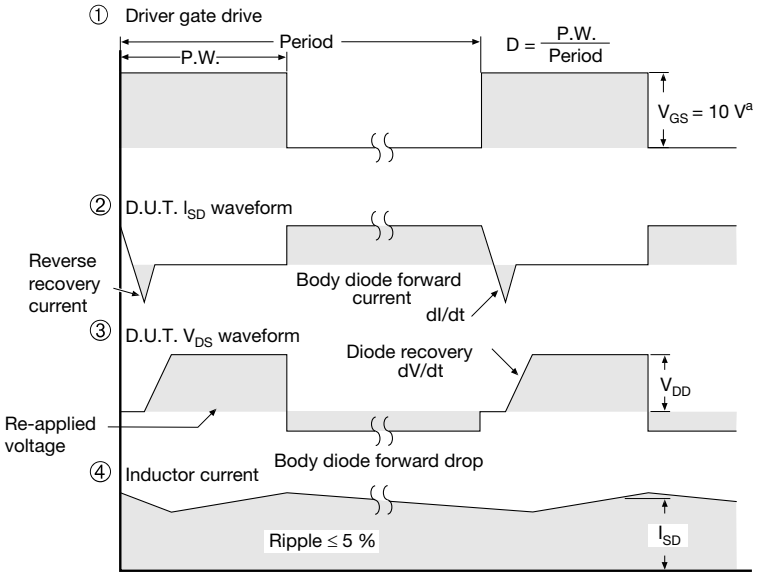


Fig. 12a - Basic Gate Charge Waveform

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 13 - For N-Channel

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