


## SCR/SCR and SCR/Diode (MAGN-A-PAK Power Modules), 170 A/250 A


**MAGN-A-PAK**

### FEATURES

- High voltage
- Electrically isolated base plate
- 3500 V<sub>RMS</sub> isolating voltage
- Industrial standard package
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL approved file E78996 
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS  
COMPLIANT**

### PRODUCT SUMMARY

$I_{T(AV)}$	170 A/250 A
Type	Modules - Thyristor, Standard
Package	MAGN-A-PAK
Circuit	Two SCRs doubler circuit

### DESCRIPTION

This new VSK series of MAGN-A-PAK modules uses high voltage power thyristor/thyristor and thyristor/diode in seven basic configurations. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or as AC-switches when modules are connected in anti-parallel mode. These modules are intended for general purpose applications such as battery chargers, welders, motor drives, UPS, etc.

### MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VSK.170..	VSK.250..	UNITS
$I_{T(AV)}$	85 °C	170	250	A
$I_{T(RMS)}$		377	555	
$I_{TSM}$	50 Hz	5100	8500	
	60 Hz	5350	8900	
$I^2t$	50 Hz	131	361	kA <sup>2</sup> s
	60 Hz	119	330	
$I^2\sqrt{t}$		1310	3610	kA <sup>2</sup> $\sqrt{s}$
$V_{DRM}/V_{RRM}$		400 to 1600	400 to 2000	V
$T_J$	Range	-40 to 130		°C



**ELECTRICAL SPECIFICATIONS**

<b>VOLTAGE RATINGS</b>				
TYPE NUMBER	VOLTAGE CODE	$V_{RRM}/V_{DRM}$ , MAXIMUM REPETITIVE PEAK REVERSE AND OFF-STATE BLOCKING VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{RRM}/I_{DRM}$ AT 130 °C MAXIMUM mA
VS-VSK.170-	04	400	500	50
	08	800	900	
	10	1000	1100	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	
VS-VSK.250-	04	400	500	50
	08	800	900	
	10	1000	1100	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	
	18	1800	1900	60
	20	2000	2100	

<b>ON-STATE CONDUCTION</b>						
PARAMETER	SYMBOL	TEST CONDITIONS		VSK.170	VSK.250	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave		170	250	A
				85	85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch		377	555	A
Maximum peak, one-cycle on-state non-repetitive, surge current	$I_{TSM}$	t = 10 ms	No voltage reappplied	5100	8500	
		t = 8.3 ms		5350	8900	
		t = 10 ms	100 % $V_{RRM}$ reappplied	4300	7150	
		t = 8.3 ms		4500	7500	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reappplied	131	361	kA <sup>2</sup> s
		t = 8.3 ms		119	330	
		t = 10 ms	100 % $V_{RRM}$ reappplied	92.5	255	
		t = 8.3 ms		84.4	233	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reappplied		1310	3610	kA <sup>2</sup> √s
Low level value or threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum)		0.89	0.97	V
High level value of threshold voltage	$V_{T(TO)2}$	(I $> \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum)		1.12	1.00	
Low level value on-state slope resistance	$r_{t1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum)		1.34	0.60	mΩ
High level value on-state slope resistance	$r_{t2}$	(I $> \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum)		0.96	0.57	
Maximum on-state voltage drop	$V_{TM}$	$I_{TM} = \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum, 180° conduction, average power = $V_{T(TO)} \times I_{T(AV)} + r_f \times (I_{T(RMS)})^2$		1.60	1.44	V
Maximum holding current	$I_H$	Anode supply = 12 V, initial $I_T = 30$ A, $T_J = 25$ °C		500	500	mA
Maximum latching current	$I_L$	Anode supply = 12 V, resistive load = 1 Ω, gate pulse: 10 V, 100 μs, $T_J = 25$ °C		1000	1000	



SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS	VSK.170	VSK.250	UNITS
Typical delay time	$t_d$	$T_J = 25\text{ }^\circ\text{C}$ , gate current = 1 A $dI_g/dt = 1\text{ A}/\mu\text{s}$ $V_d = 0.67\% V_{DRM}$	1.0		$\mu\text{s}$
Typical rise time	$t_r$		2.0		
Typical turn-off time	$t_q$	$I_{TM} = 300\text{ A}$ ; $dI/dt = 15\text{ A}/\mu\text{s}$ ; $T_J = T_J$ maximum; $V_R = 50\text{ V}$ ; $dV/dt = 20\text{ V}/\mu\text{s}$ ; gate 0 V, 100 $\Omega$	50 to 150		

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS	VSK.170	VSK.250	UNITS
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = T_J$ maximum	50	60	mA
RMS insulation voltage	$V_{INS}$	50 Hz, circuit to base, all terminals shorted, 25 $^\circ\text{C}$ , 1 s	3000		V
Critical rate of rise of off-state voltage	$dV/dt$	$T_J = T_J$ maximum, exponential to 67 % rated $V_{DRM}$	1000		V/ $\mu\text{s}$

TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS	VSK.170	VSK.250	UNITS
Maximum peak gate power	$P_{GM}$	$t_p \leq 5\text{ ms}$ , $T_J = T_J$ maximum	10.0		W
Maximum average gate power	$P_{G(AV)}$	$f = 50\text{ Hz}$ , $T_J = T_J$ maximum	2.0		
Maximum peak gate current	+ $I_{GM}$	$t_p \leq 5\text{ ms}$ , $T_J = T_J$ maximum	3.0		A
Maximum peak negative gate voltage	- $V_{GT}$	$t_p \leq 5\text{ ms}$ , $T_J = T_J$ maximum	5.0		V
Maximum required DC gate voltage to trigger	$V_{GT}$	$T_J = -40\text{ }^\circ\text{C}$	4.0		
		$T_J = 25\text{ }^\circ\text{C}$	3.0		
		$T_J = T_J$ maximum	2.0		
Maximum required DC gate current to trigger	$I_{GT}$	$T_J = -40\text{ }^\circ\text{C}$	350		mA
		$T_J = 25\text{ }^\circ\text{C}$	200		
		$T_J = T_J$ maximum	100		
Maximum gate voltage that will not trigger	$V_{GD}$	$T_J = T_J$ maximum, rated $V_{DRM}$ applied	0.25		V
Maximum gate current that will not trigger	$I_{GD}$	$T_J = T_J$ maximum, rated $V_{DRM}$ applied	10.0		mA
Maximum rate of rise of turned-on current	$dI/dt$	$T_J = T_J$ maximum, $I_{TM} = 400\text{ A}$ , rated $V_{DRM}$ applied	500		A/ $\mu\text{s}$

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	VSK.170	VSK.250	UNITS
Junction operating and storage temperature range	$T_J$ , $T_{Stg}$		- 40 to 130		$^\circ\text{C}$
Maximum thermal resistance, junction to case per junction	$R_{thJC}$	DC operation	0.17	0.125	K/W
Typical thermal resistance, case to heatsink per module	$R_{thCS}$	Mounting surface flat, smooth and greased	0.02	0.02	
Mounting torque $\pm 10\%$	MAP to heatsink busbar to MAP	A mounting compound is recommended and the torque should be rechecked after a period of about 3 hours to allow for the spread of the compound.	4 to 6		Nm
Approximate weight			500		g
			17.8		oz.
Case style			MAGN-A-PAK		



<b>ΔR CONDUCTION PER JUNCTION</b>											
DEVICES	SINUSOIDAL CONDUCTION AT T <sub>J</sub> MAXIMUM					RECTANGULAR CONDUCTION AT T <sub>J</sub> MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSK.170-	0.009	0.010	0.010	0.020	0.032	0.007	0.011	0.015	0.020	0.033	K/W
VSK.250-	0.009	0.010	0.014	0.020	0.032	0.007	0.011	0.015	0.020	0.033	

**Note**

- Table shows the increment of thermal resistance R<sub>thJC</sub> when devices operate at different conduction angles than DC

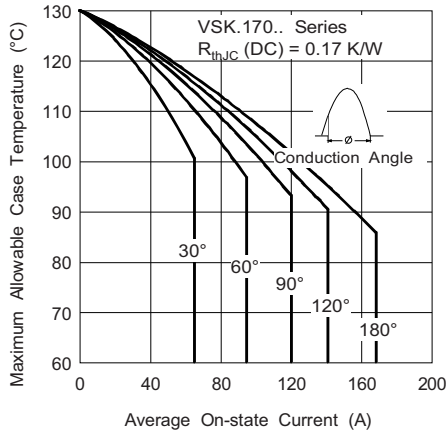


Fig. 1 - Current Ratings Characteristics

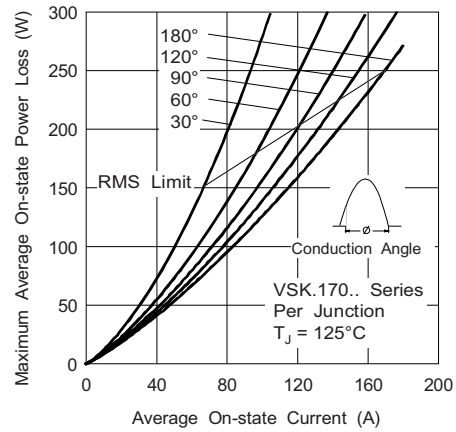


Fig. 3 - On-State Power Loss Characteristics

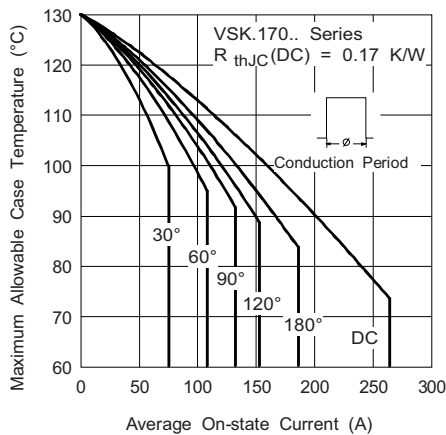


Fig. 2 - Current Ratings Characteristics

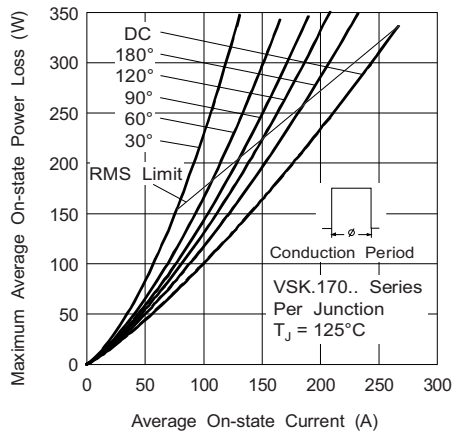


Fig. 4 - On-State Power Loss Characteristics

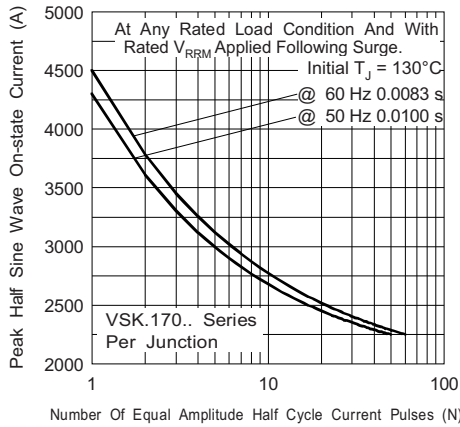


Fig. 5 - Maximum Non-Repetitive Surge Current

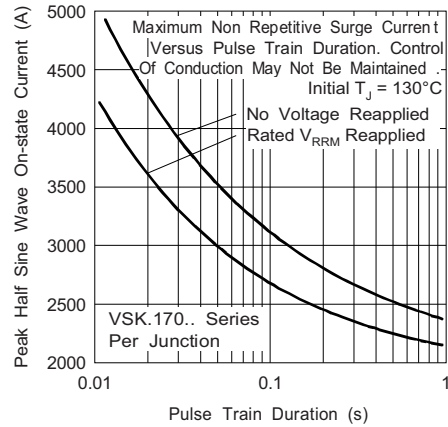


Fig. 6 - Maximum Non-Repetitive Surge Current

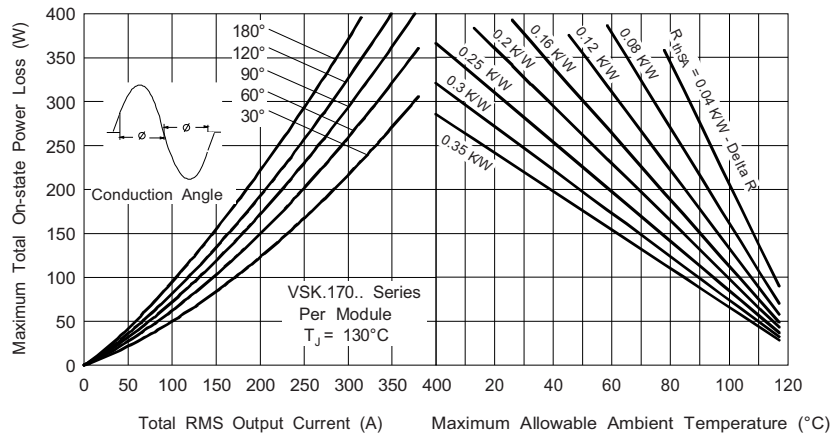


Fig. 7 - On-State Power Loss Characteristics

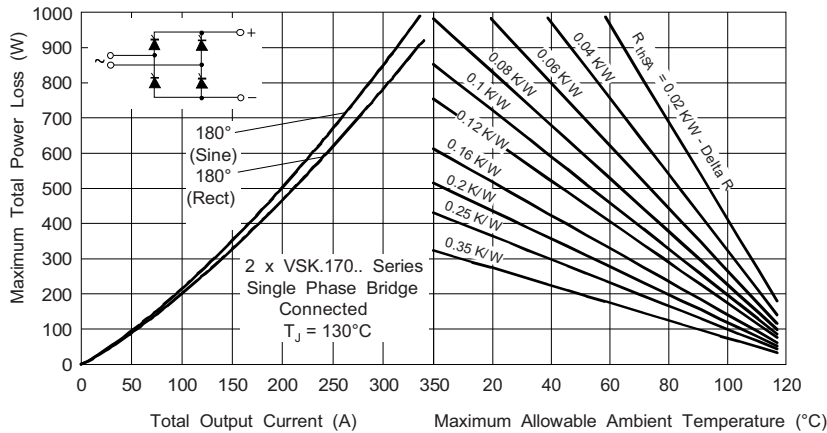


Fig. 8 - On-State Power Loss Characteristics

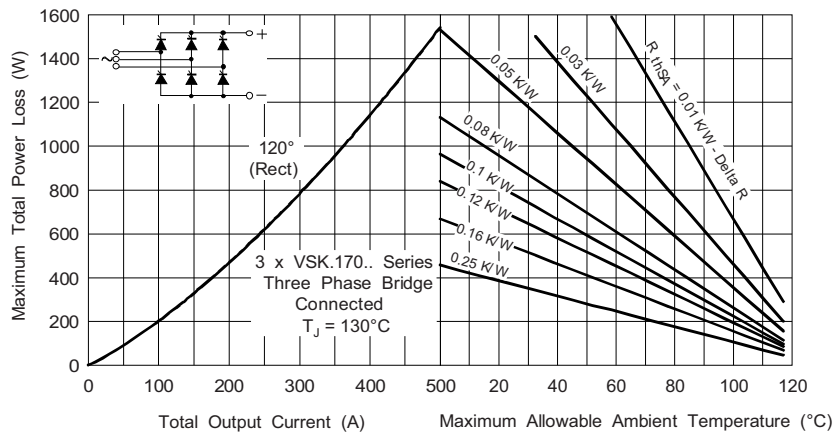


Fig. 9 - On-State Power Loss Characteristics

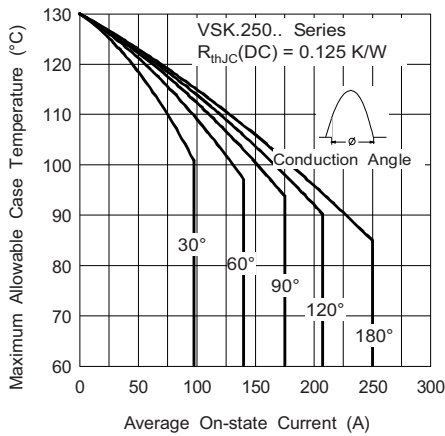


Fig. 10 - Current Ratings Characteristics

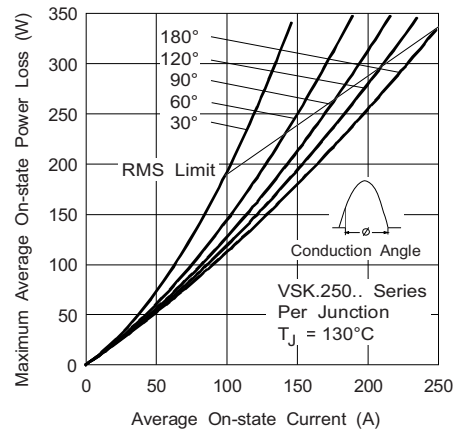


Fig. 12 - On-State Power Loss Characteristics

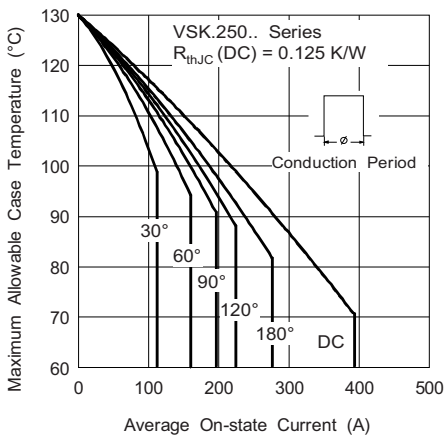


Fig. 11 - Current Ratings Characteristics

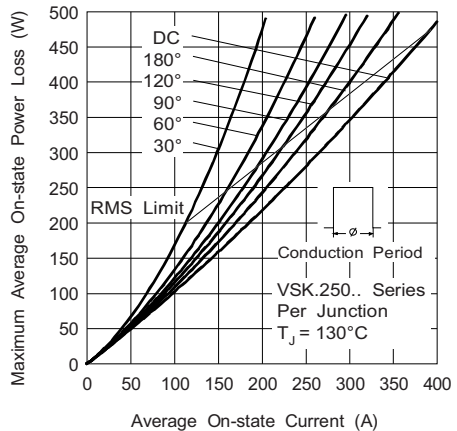


Fig. 13 - On-State Power Loss Characteristics

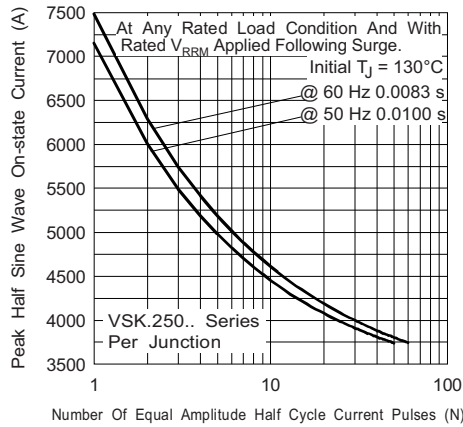


Fig. 14 - Maximum Non-Repetitive Surge Current

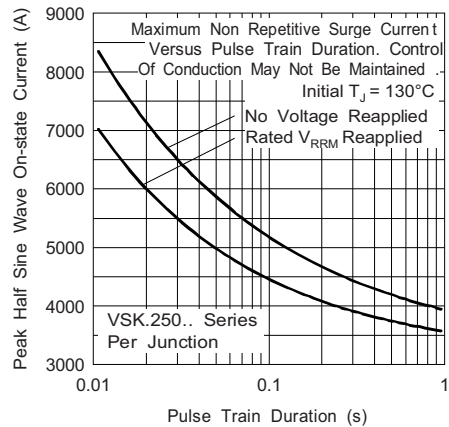


Fig. 15 - Maximum Non-Repetitive Surge Current

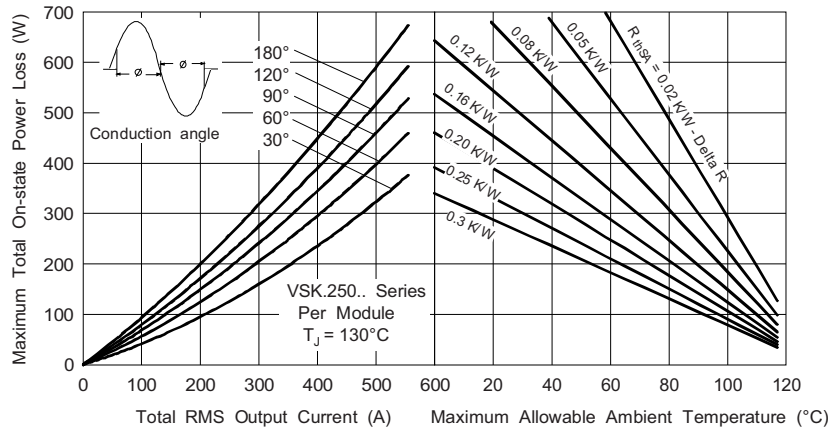


Fig. 16 - On-State Power Loss Characteristics

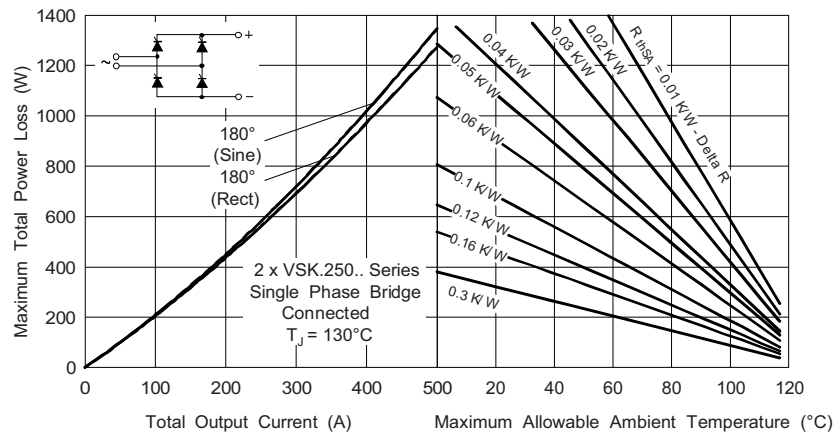


Fig. 17 - On-State Power Loss Characteristics

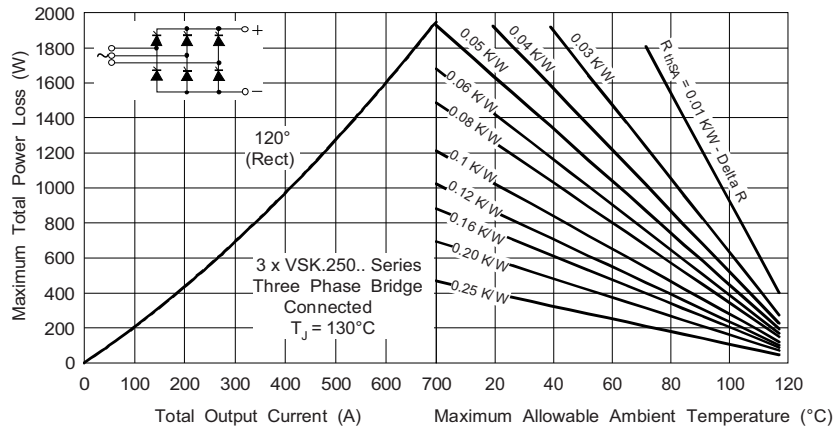


Fig. 18 - On-State Power Loss Characteristics

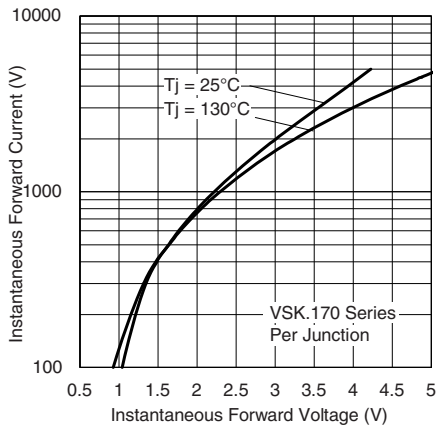


Fig. 19 - On-State Voltage Drop Characteristics

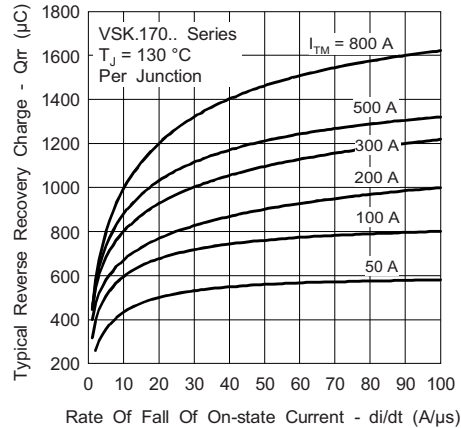


Fig. 21 - Reverse Recovery Charge Characteristics

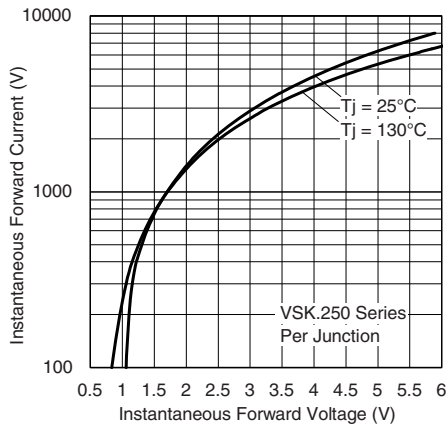


Fig. 20 - On-State Voltage Drop Characteristics

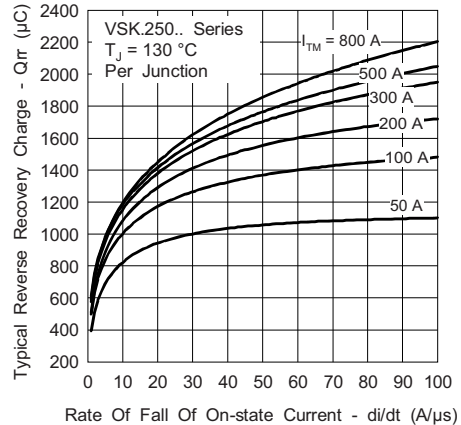


Fig. 22 - Reverse Recovery Charge Characteristics



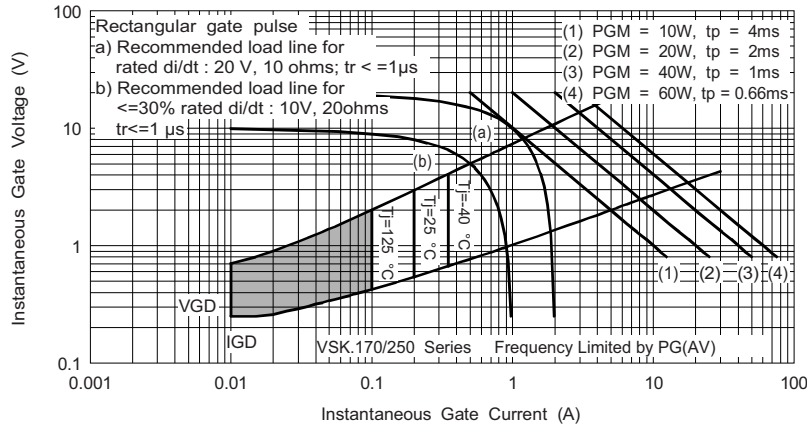


Fig. 23 - Gate Characteristics

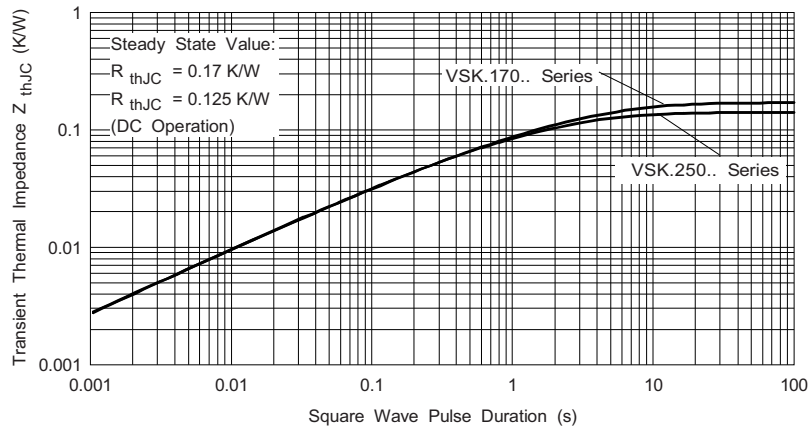


Fig. 24 - Thermal Impedance Z<sub>thJC</sub> Characteristics

**ORDERING INFORMATION TABLE**

Device code	<b>VS-VS</b>	<b>KT</b>	<b>250</b>	<b>-</b>	<b>20</b>	<b>PbF</b>
	①	②	③		④	⑤

- 1** - Vishay Semiconductors product
- 2** - Circuit configuration (see dimensions - link at the end of datasheet)
- 3** - Current rating
- 4** - Voltage code x 100 = V<sub>RRM</sub> (see voltage ratings table)
- 5** -
  - None = standard production
  - PbF = lead (Pb)-free

**Note**

- To order the optional hardware go to [www.vishay.com/doc?95172](http://www.vishay.com/doc?95172)



CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs doubler circuit	KT	<p>Available from 400 V to 1600 V for VSK.170PbF Series, available from 400 V to 2000 V for VSK.250PbF Series</p>
SCR/diode doubler circuit, positive control	KH	<p>Available from 400 V to 1600 V for VSK.170PbF Series, available from 400 V to 2000 V for VSK.250PbF Series</p>
SCR/diode doubler circuit, negative control	KL	<p>Available from 400 V to 1600 V for VSK.170PbF Series, available from 400 V to 2000 V for VSK.250PbF Series</p>
Two SCRs common cathodes	KU	<p>Available up to 1200 V, contact factory for different requirement</p>
Two SCRs common anodes	KV	<p>Available up to 1200 V, contact factory for different requirement</p>

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95086">www.vishay.com/doc?95086</a>

## MAGN-A-PAK

**DIMENSIONS** in millimeters (inches)



### Notes

- Dimensions are nominal
- Full engineering drawings are available on request
- UL identification number for gate and cathode wire: UL 1385
- UL identification number for package: UL 94 V-0



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